

SOSATM SPECIAL EDITION

Sensor Open Systems Architecture

2022 | Volume 2 | Number 1

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2022



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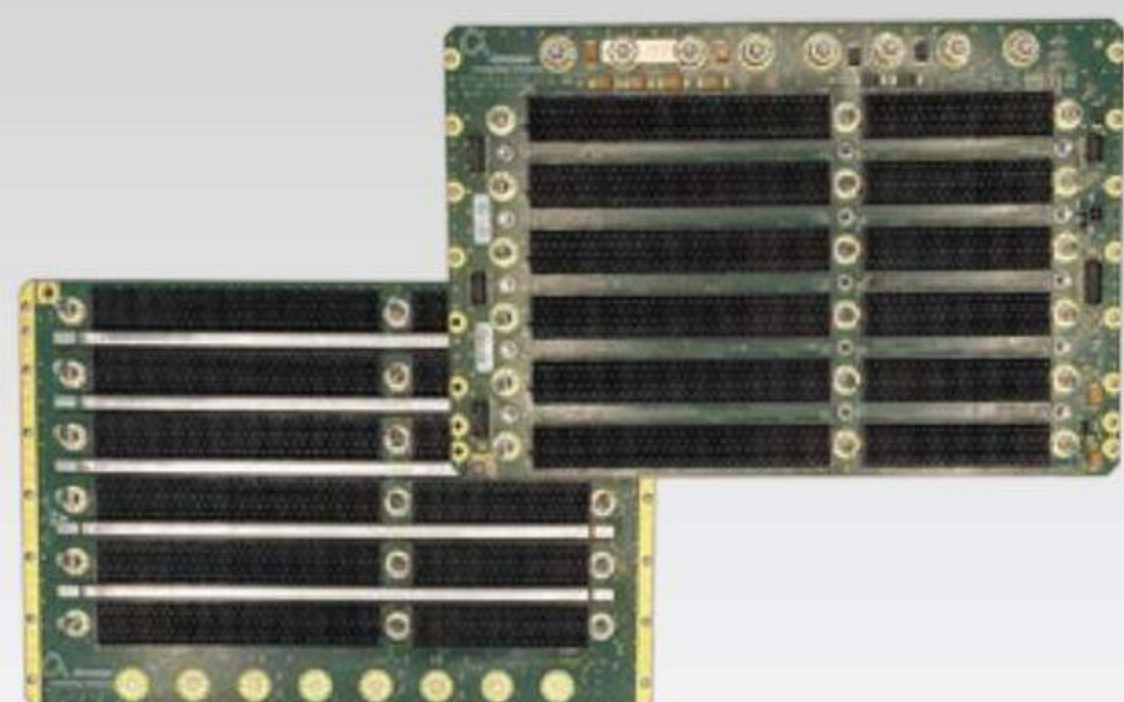


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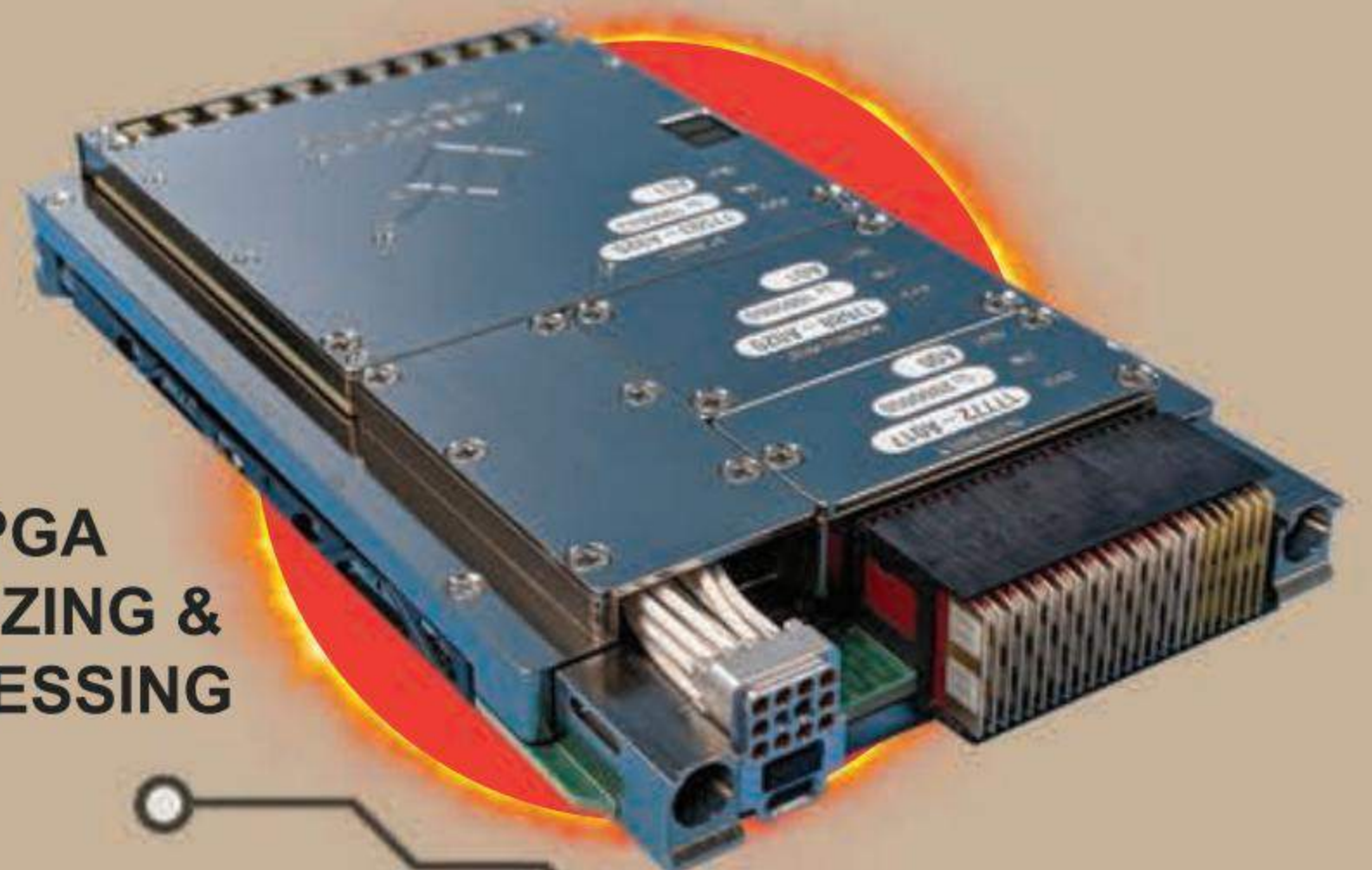
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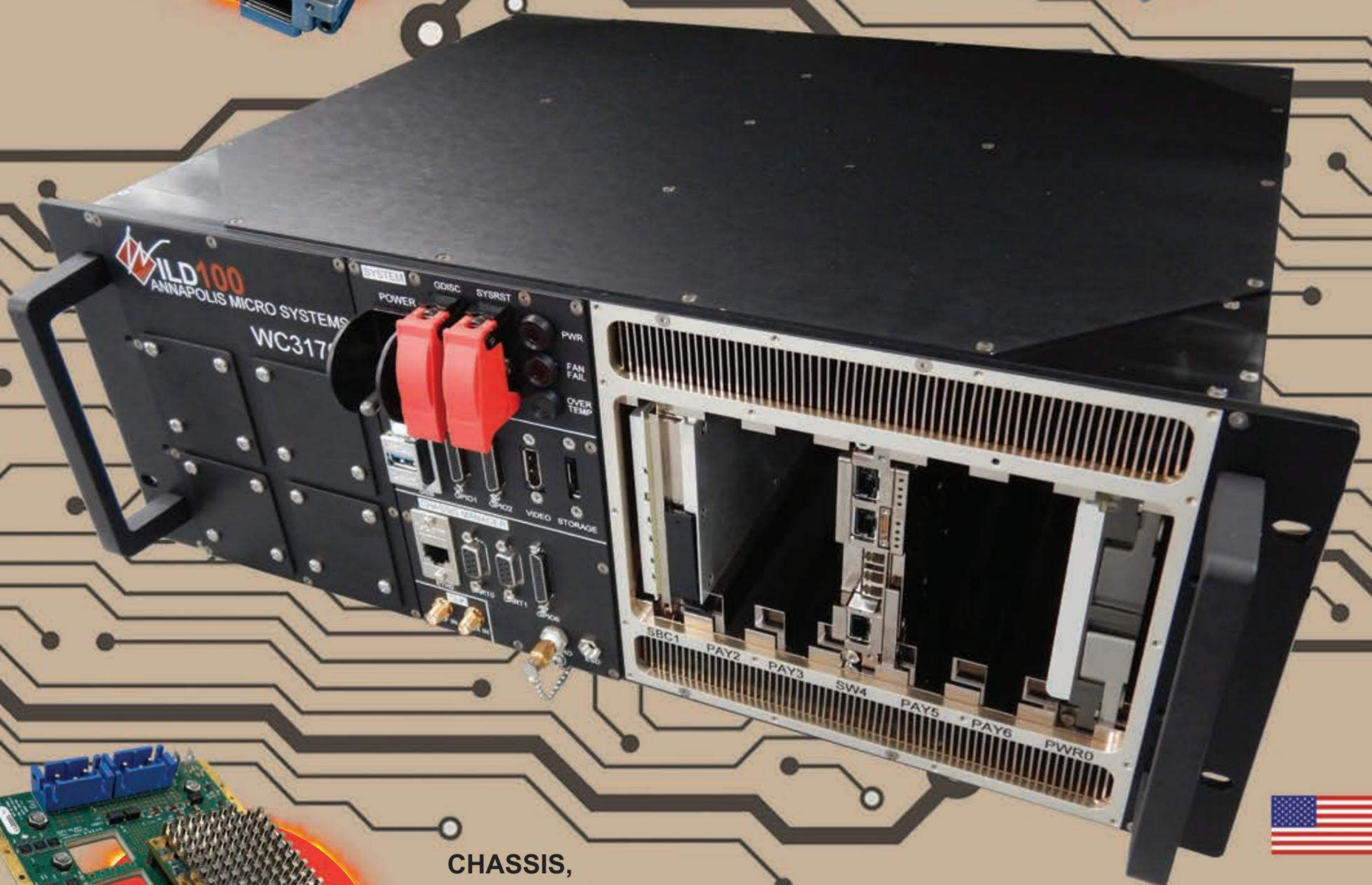
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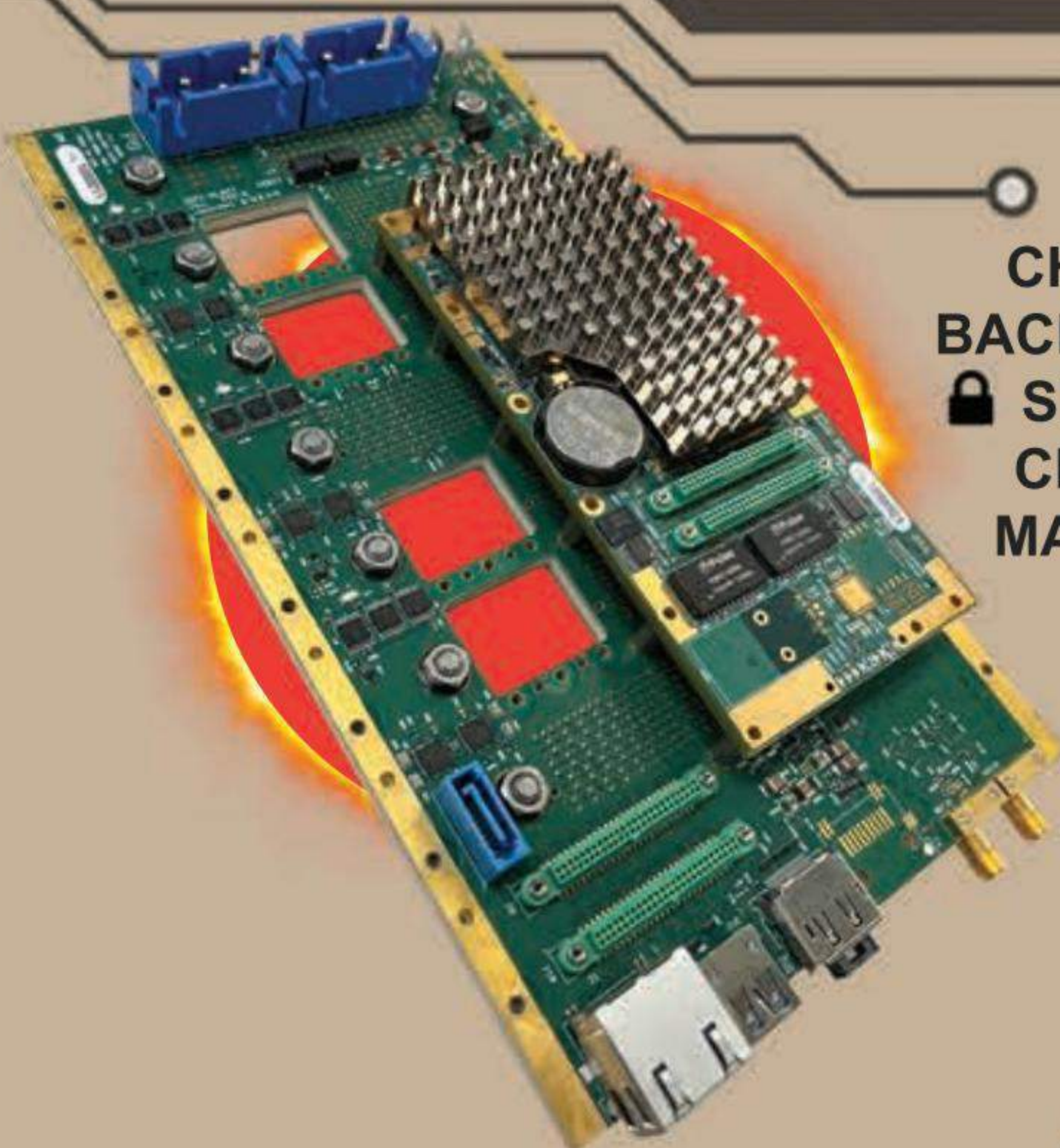


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ON THE COVER

An XQ-58A Valkyrie unmanned aerial vehicle (UAV) launches during a test at the U.S. Army Yuma Proving Ground in Arizona. The acquisition and testing team was comprised of Air Force Research Laboratory and Air Force Life Cycle Management Center personnel working together with the Eglin Air Force Base (Florida) 46th Test Squadron. The platform pictured is under development with key systems designed to be in alignment with The Open Group's SOSA [Sensor Open Systems Architecture] Technical Standard. (U.S. Air Force photo/Staff Sgt. Joshua King.)



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The SOSA Technical Standard leverages and complements open standards in government and industry. It defines architectural modules (containing functions and behaviors) with defined open interfaces, enabling the development of capabilities made up of common components. The standard incorporates specifications for software components and hardware elements, as well as electrical and mechanical interfaces composing the SOSA sensor element.

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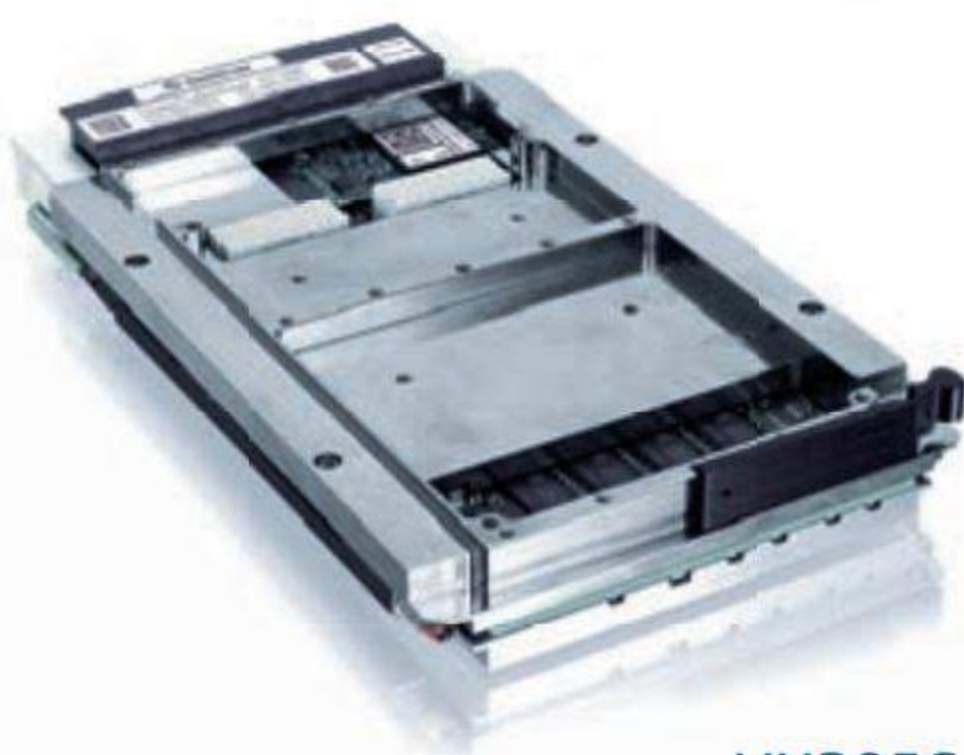
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Editor's Perspective

By John McHale, Editorial Director

SOSA and MOSA momentum

Welcome to the SOSA Special Edition 2022, our second of what is an annual issue highlighting editorial content on The Open Group's Sensor Open Systems Architecture (SOSA) Technical Standard from the pages and website of Military Embedded Systems Magazine, as well as the products aligned and conformant to the technical standard – all put together exclusively by our staff.

Almost a year has passed since the release of the SOSA Technical Standard Reference Architecture, Edition 1.0, with momentum continuing to grow as more programs begin requiring SOSA aligned solutions in future systems designs and technology upgrades.

Fueling that momentum is the continued push by the end user – the U.S. Department of Defense (DoD) – for new systems and upgrades to leverage open architectures in designs. This push was mandated in 2019 in the so-called Tri-Service Memo from the U.S. Air Force, Army, and Navy leadership, which asserted that “Modular Open Systems Approaches for our weapon systems is a warfighting imperative.” The joint document stated that “development of a modular open systems approach (MOSA) in areas where we lack them is vital to our success.” The memo mentioned SOSA, FACE [Future Airborne Capability Environment], and other standards by name as examples of MOSA.

“MOSA is near and dear to my heart, [I’m] very passionate about it. We cannot continue to integrate independent, self-contained solutions within our platform any longer,” said Giorgio Bertoli, Assistant Director for the Spectrum Dominance and Intelligence portfolio within the U.S. Army's C5ISR Center, in his keynote address “C5ISR/EW Modular Open Suite of Standards (CMOSS) ‘The

Army's SOSA Instantiation’” at our MOSA Virtual Summit in February. “C5ISR moves too fast to possibly think you can follow a standard acquisition process where you buy a turnkey black-box system that will sustain you for the next 10-20 years – it just can't happen.”

Whether due to mandates or passion, in any case the momentum for MOSA strategies like SOSA and CMOSS is increasing across multiple areas of the U.S. military. When I asked Jim Smith, Acquisition Executive for U.S. Special Operations Command (USSOCOM), about open architectures at a press briefing at the Special Operations Forces Industry Conference (SOFIC) in Tampa, he told me: “It's embedded in our acquisition strategy and the reason for that is that SOCOM being a joint force needs to be interoperable with the [other services].”

Smith said that SOCOM quite likes the SOSA Technical Standard, especially for what it means for counter-UAS [unmanned aerial system] applications. These systems are designed to deal with multiple threats and will need an open architecture that can work with more than one sensor, he added.

SOSA's effect on UAS and counter-UAS applications is also related to how SOSA is influencing the development of small-form-factor standards, as detailed in the article titled “Unmanned ISR payloads leverage MOSA designs,” on page 20.

“A lot of SOSA is built on VITA standards and OpenVPX. OpenVPX is currently 3U and 6U plug-in cards, but there are new smaller-form-factor VPX standards that are emerging,” says Rodger Hosking, director of sales, Mercury (Upper Saddle River, New Jersey), in the article. “Once they become a standard in VITA, SOSA

will then adopt the best of those standards and incorporate them under the SOSA specification. SOSA doesn't like to invent its own standards; what it likes to do is choose from the best standards that are out there, pick the best parts, and then say these are the parts that will be in the SOSA standard.”

A common misconception about SOSA is that it only focuses on sensor systems. Not so: It also provides for mission-compute applications. This means that SOSA will apply not only to the RF portion of a radar system but also to the processor box. This fact is evident with the work being done with small form factors as well as on 3U VPX and 6U VPX.

In addition to looking at small-form-factor adoption, the SOSA Consortium is also studying how to apply SOSA to space applications. An example of open standard designed for space – SpaceVPX – is detailed on page 46 in the article titled “Standards-driven innovation: A perspective on SpaceVPX.”

As the SOSA Consortium adopts new standards into the SOSA Technical Standard it is also adding new members, with the current organization roster up to 137. For examples of member solutions and products, be sure to refer to our Product Profile section, starting on page 58.

This edition, nor last year's inaugural one, could have happened without the help and cooperation of Reggie Hammond and her colleagues at The Open Group, as well as the SOSA Outreach Committee co-chairs – Valerie Andrew of Elma Electronic and Gina Peter of Pentek, now a part of Mercury Systems. Many thanks for your help on this second iteration of the SOSA Special Edition.

SOSA interview with C. Patrick Collier



C. Patrick Collier

Below are updated excerpts from an interview previously conducted by The Open Group with C. Patrick Collier, co-founder of SOSA and chair of the Hardware Working Group. For the full interview, visit <https://www.opengroup.org/collier/sosa>.

How did you first become involved in The Open Group SOSA Consortium?

COLLIER: I started my career at the AFRL Research Space Vehicles Directorate at Kirtland AFB, Albuquerque, New Mexico. With respect to how I first became involved with standards, I was a co-founder of an effort called Next Generation Space Interconnect Standards (NGSIS) with a colleague from NASA JPL, an umbrella organization that developed two separate standards. One was called SpaceVPX. SpaceVPX became a base-line standard for all space applications, like an OpenVPX for terrestrial applications.

The other standard was the RapidIO Space Device Class. This was an effort with the RapidIO Trade Association. Just like SOSA, the NGSIS/SpaceVPX/RapidIO Space Device Class efforts had input from both government and industry.

When you first met [SOSA steering committee chair Dr.] Ilya Lipkin, was he already involved?

COLLIER: I first met Ilya while I was with the AFRL Space Vehicles Directorate, Kirtland AFB. After Ilya got involved, we began work on the first documents that would become SOSA. Others from the Air Force, Army, and Navy were also involved, including Bob Matthews from NAVAIR, John Bowling from the Air Force, Ben Peddicord, and Jason Dirner from Army CMOSS. We interacted with the FACE Consortium and set up the SOSA Consortium to incubate under The Open Group FACE Consortium.

After that, [interest and momentum] started to build so we did a kickoff for the SOSA Technical Standard. All the services were represented at the kickoff because everybody was already doing HOST, CMOSS, FACE, and other standards work together, so we agreed to work together rather than do things independently.

Were there models of how other standards had approached conformance that inspired your approach, or did you start with a clean slate?

COLLIER: It's a little bit of both. The Open Group person who was helping us do hardware was also involved in the FACE Consortium, so initially we looked at whether The Open Group had a conformance

verification/certification process in place. They did for the FACE Consortium, and we are basically using that same process. The SOSA Conformance process does differ somewhat from the FACE Conformance with respect to the template, because FACE involves software only. With the SOSA Conformance, we have hardware pieces to verify and certify. There's a vast difference in terms of the responsibility for verifying and certifying hardware versus software.

One example is the challenge of setting up a Verification Authority that can verify different types of hardware, whether it's a plug-in card, or another type of hardware element, which can be anything. If somebody has an entire subsystem they want to incorporate, it necessitates the SOSA Conformance process be quite different than that used by the FACE Conformance. In that sense, we are starting from a clean slate, at least regarding how The Open Group was doing the FACE Conformance.

How do you refer to the SOSA Conformance process – is it a plan?

COLLIER: Yes, you can call it a plan. More appropriately, we refer to it as a program. There are different pieces to it. There's a policy document that provides some guidance, but there's also a Conformance Guide, which explains in detail how to prepare a candidate system or component for verification and then certification.

One of the criticisms against OpenVPX, as successful as it's been, is that it was an open standard that allowed suppliers to define their own profiles. Since vendors naturally have the tendency to look out for their self-interest, how did you ensure that the SOSA Technical Standard would not replicate that history?

COLLIER: From a hardware perspective, industry was already invested in using VITA standards and developing products based on those standards. VITA actually started with the Army and the Navy, but eventually everyone adopted VITA since that's what industry was using. The approach we took was to reflect on those things that are important to us. What you see in the standard focuses on technical principles and quality attributes. We wanted to down-select to a subset of profiles that would maximize the interchangeability or portability of the SOSA building blocks. That ensures the ability to take a given hardware component and reuse it for another application.

We actively discussed the extent to which you can actually plug and play components because there are limits. We had to consider exactly what one would have to do in order to reuse a component. The intent was to reduce the amount of user-defined space in the profiles. With OpenVPX, having a lot of available user-defined space provides flexibility for a supplier to say "OK, I can take this user-defined space and put signals on it that will help a certain application." In doing that, however, you limit the utility of that hardware to a custom application. The result is that reuse goes down. We did a trade study to explore how to maximize reuse; one of the ways is to reduce user-defined space, specifically in profiles.

That finding informed the hardware section of the SOSA Technical Standard. None of the profiles, except for two that were included for specific reasons, have any user-defined space. The SOSA profiles were designed or developed that way so that the government can take a SOSA component – for example, a plug-in card from a profile that has a VITA slot profile – and readily reuse it for another application. Granted, it may be necessary to do some reconfiguration, and that's where conformance comes in. It makes it possible to verify that a supplier has adhered to the standard, which in turn means adhering to the interface definitions for those profiles.

Now a government customer can say, "I have this profile and it's supposed to do this and this, and I can put it here in this application, but I also know I can also use it somewhere else because the interfaces are similar or the same".

Did you have to battle the desire to create areas of special dispensation and exemption and still claim conformance?

COLLIER: That's another benefit of the SOSA Consortium, where both industry and government are involved. We worked the problem together and everybody agreed to share some of the pain. We agreed that reducing flexibility increases interchangeability and portability. As a result, industry is incentivized to optimize the most prevalent interfaces they currently use or think they or the government will need to use. There was a constant conversation and a lot of work that went into making those decisions. Granted, a lot of the profiles in the standard were baselined from some that were already works in progress by the Army.

With that in mind, discussions focused on establishing consensus regarding the types of profiles and their interfaces. Those conversations are still going on today, especially on some of the interfaces and protocols. There's a lot of discussion about what makes the most sense and how to make the best use of those profiles. And conformance is going to make sure we can verify that a supplier properly used those interfaces in creating a product.

So, basically, the philosophy was, there's an onus, in that vendors are going to sacrifice the ability to have uniqueness, but the bonus is the wider market opportunity because they'll make it up in volume, arguably?

COLLIER: Yes, that's one of the reasons why you see the services wanting to do this together, to increase those economies of scale. Uniqueness is defined inside the SOSA components, not at the interfaces.

Do you envision a distinction between verification and certification? Might companies self-verify or does that require a third party?

COLLIER: The way it will run is there will be third-party VAs [verification authorities] that will collect information from a supplier and perform verification. The nice thing is that the people involved in the Consortium – for example those in a software environment or security subcommittee – will develop the conformance methodologies that the VA will use to inspect, analyze, test, and/or demonstrate that the product comports with the standard. The subcommittee experts will have a voice in what makes the most sense. Then the VA, which is an independent organization, will execute those conformance methodologies.

Once the verification process is finished, the product goes to a certification body run by The Open Group. The certification body will conduct the requisite checks required to declare the product “SOSA conformant.”

What are the most common questions that you get asked about the conformance process?

COLLIER: There are a lot of questions about the cost of conformance and the cost of verification, because there’s a concern that it will be too expensive to get a product certified. The certification process will have a flat fee. The cost of verification, according to The Open Group, will be by agreement between the product supplier and the VA. I get a lot of financial questions, and a lot of questions about verification matrices and associated procedures.

People want to understand “how would you verify this?” because there will need to be conversations between matrix developers and a potential VA. We get questions about external standards and how to execute requirements from an external standard, because, according to The Open Group, we have to account for those cases. There are also a lot of questions about how we plan to phase in the conformance program. Right now, we are phasing in the program because of limited resources.

We need to build an understanding of what industry might bring in for verification, because companies are already developing products. We are looking for the lowest-hanging fruit to address first, to get the program off the ground and running. The challenges are that we have to go through all those gates and get funding for test tool development and VA certification. We can’t do anything without adequate resources. Those are some of the most common questions we’ve heard over the past few months.

Do you have a sense of timing in regards to when suppliers will be able to offer certified products?

COLLIER: The SOSA Conformance Standing Committee is working to begin the SOSA Conformance Program by the end of calendar year 2022.

Will there be a database of certified products that is maintained by The Open Group?

COLLIER: The Open Group Certification Authority will maintain a database – a Certification Registry – for all SOSA certified sensor components.

What would you say has been the greatest satisfaction that you’ve derived from your role and participation in the SOSA process?

COLLIER: I’d say just being able to help develop the SOSA Technical Standard and contribute content for an important standard. Also, it’s been gratifying to help others who are involved get over hurdles they encounter while working to develop and refine content. For me, seeing SOSA v1.0 published is a huge accomplishment, because as the SOSA Technical Standard transitions from a “snapshot” into an official standard, it becomes a real thing. ■

***C. Patrick Collier** is co-founder of SOSA and chair of the hardware subcommittee and conformance standing committee. Patrick also founded and is currently chair for the VITA 78 (SpaceVPX) and VITA 78.1 (SpaceVPX Lite) standards undertakings. He is a senior open systems engineer with Aspen Consulting Group.*



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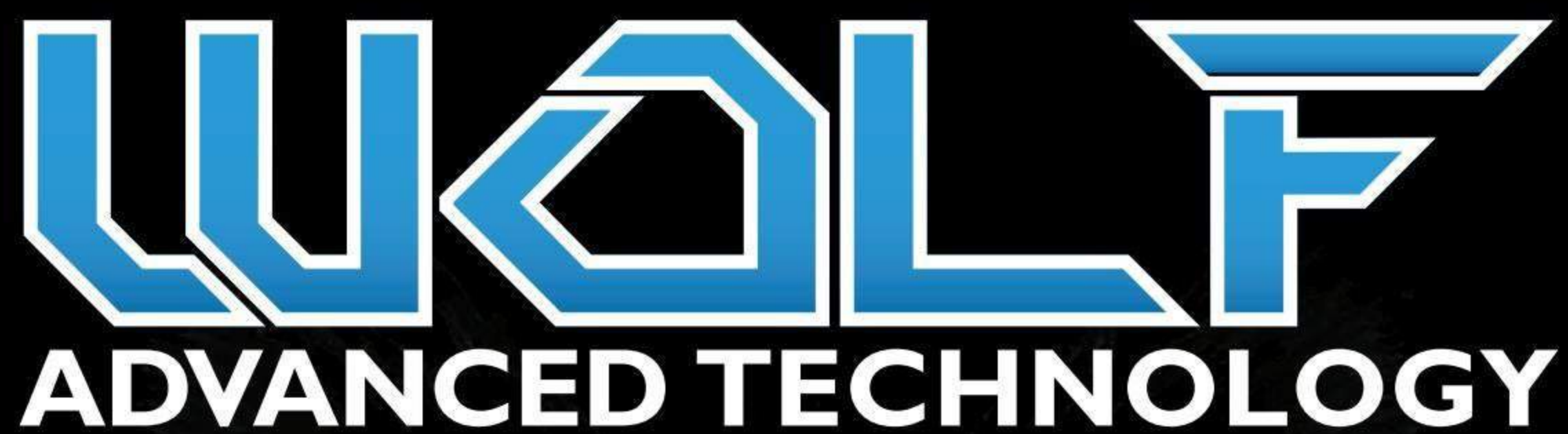
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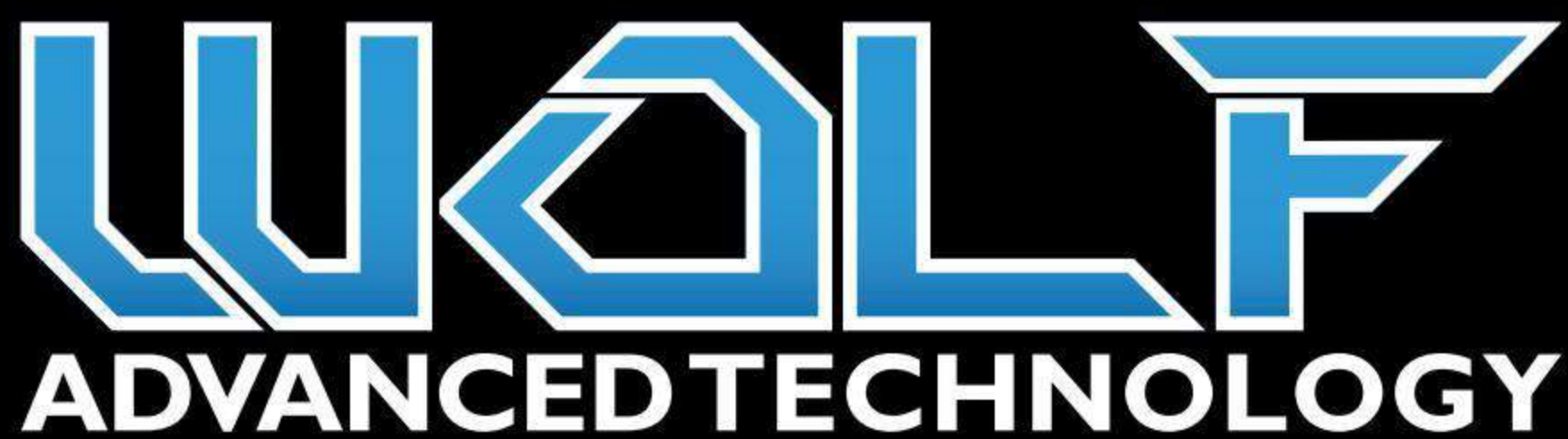
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 - SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13
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 - SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 (SBC)
 - SLT3-PAY-SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11/14.6.13 (Payload)

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AV67.3 Coax for SDI and CVBS output,
SOSA™ Aligned Payload Profile (WOLF-1349)**



- ▶ NVIDIA Turing, 9.5 TFLOPS peak, WOLF FGX video conversion, PCIe Gen4 switch
- ▶ Integrate, demonstrate, deploy and upgrade sensor data processing efficiently with SOSA and AV67.3 coaxial connections. Tune power and PCIe topologies to reduce slot count and increase overall system efficiency. Deploy HPC and AI processing for EW, ISR and data processing. This 3U VPX module includes a new Interface Control Document (ICD) that includes factory configurable options which can be used to maintain compliance with many Open COTS initiatives. By default the module has been designed to support SOSA Payload slot profile:
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Unmanned ISR payloads leverage MOSA designs

By Emma Helfrich



An unmanned aerial vehicle delivers a payload to the Ohio-class ballistic-missile submarine USS Henry M. Jackson near the Hawaiian Islands. U.S. Navy photo by Mass Communication Specialist 1st Class Devin M. Langer.

See more, detect more, and decode more – these are the primary requirements being asked of unmanned systems in the military, and proprietary hardware and software can make achieving those goals a challenge. This is why Army, Navy, and Air Force leaders mandated a Modular Open Systems Approach (MOSA) for all new programs and upgrades. MOSA examples include The Open Group’s Sensor Open Systems Architecture (SOSA) Technical Standard and the Future Airborne Capability Environment (FACE) Technical Standard. These initiatives among others, aim to offer commonality of hardware to enable easier and more affordable technology insertion in unmanned systems.

The U.S. Department of Defense (DoD) is looking to acquire more information from the field than ever before, thus requiring sensors to be increasingly capable even as the electromagnetic spectrum (EMS) grows more crowded. The sensor payloads of unmanned platforms – unmanned aerial vehicles (UAVs), unmanned ground vehicles (UGVs), and unmanned underwater vehicles (UUVs) – carry much of that data-gathering pressure and expectation.

With the varying size, operating environment, and overall mission architecture of

these unmanned systems, timely and cost-efficient technology refresh can prove to be difficult. This need also affects the control station operating the unmanned systems, as standardizing on communication ports has the potential to increase bandwidth and create opportunities for stronger information processing.

Between the potential for extended life cycles, lower acquisition costs, and better enabling of multidomain operations, adopting open architecture standards on unmanned platforms is gaining global attention, as well. With Joint All-Domain Command and Control (JADC2) at the forefront of DoD efforts, NATO allies are taking note of the positive effects open standards could have on joint-domain operations.

At this point in the evolution of open standards as they relate to the specific needs of an unmanned platform, industry officials are confident that any prospective drawbacks of one standard could be addressed and resolved by another. With size a prominent characteristic of UAVs, establishing a standard for small-form-factor (SFF)

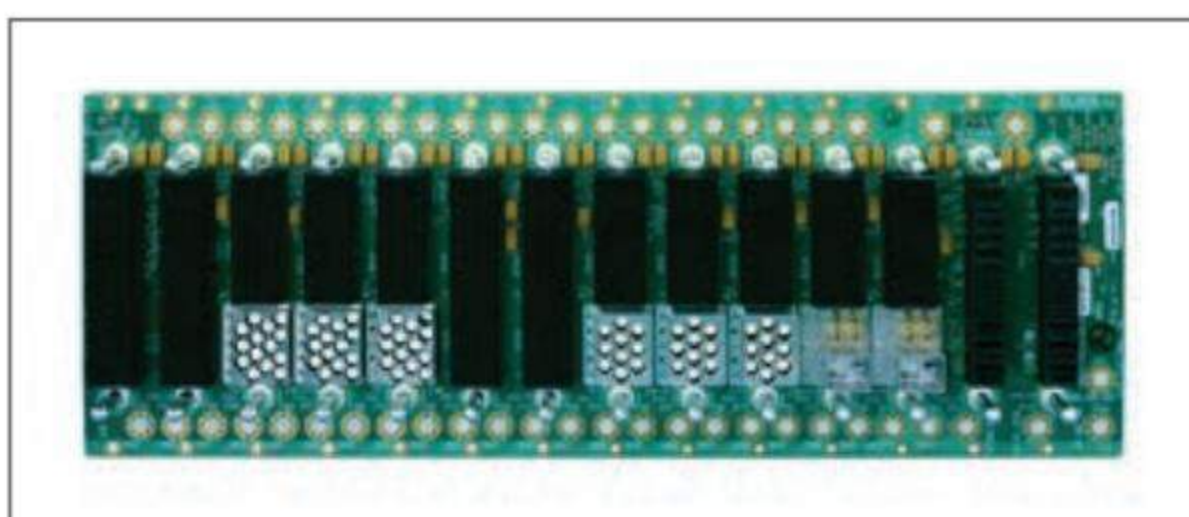


FIGURE 1 | Elma Electronic's 3U 12-slot backplane is aligned to SOSA as well as the latest iteration of CMOSS [C5ISR/EW Modular Open Suite of Standards] requirements, developed specifically for the U.S. Army. Among the supported profiles are two switch slots (center), a timing (PNT) slot, and two slots for VITA 62 compliant power supply modules (far right).

sensor payloads is in the works for standards organizations.

Standardizing SFF

There do exist standards currently in use that are dedicated to creating hardware for smaller platforms. The VITA Standards Organization (VSO) offers 3U OpenVPX and 6U OpenVPX, but for unmanned systems that may eventually call for thimble-sized electronics, the standardization timeline will be dependent on adoption by SOSA.

"A lot of SOSA is built on VITA standards and OpenVPX. OpenVPX is currently 3U and 6U plug-in cards, but there are new smaller form factor VPX standards that are emerging," says Rodger Hosking, director of sales, Mercury, Upper Saddle River, New Jersey. "As those emerge, what will happen is once they become a standard in VITA, SOSA will then adopt the best of those standards and incorporate them under the SOSA specification. SOSA doesn't like to invent its own standards; what it likes to do is choose from the best standards that are out there, pick the best parts, and then say these are the parts that will be in the SOSA standard. Smaller designs will come about in SOSA when they come about in VITA."

Developing open standards for small unmanned aircraft platforms is critical goal of the U.S. Army. The Army is "very big on UASs [unmanned aircraft systems] from Category 5 to Category 1. [Category 5 is the largest and Category 1 is the smallest.] You cannot fit OpenVPX on anything below Category 3," says Giorgio Bertoli, Assistant Director for the Spectrum Dominance and Intelligence portfolio within the U.S. Army's C5ISR Center, during his keynote address at the MOSA Virtual Summit titled "C5ISR/EW Modular Open Suite of Standards (CMOSS) 'The Army's SOSA Instantiation.'"

"However, there are other options," he continues. "One is the new VNX option, much smaller but highly capable and incredibly light and can easily fit on even a Category 1 UAS. We also have a tiny chassis that can fit these little cards and still support modular open system approaches." Bertoli notes that he sees VNX as the "closest viable platform for a SOSA SFF." To view his entire presentation, visit https://www.bigmarker.com/series/mosa-virtual-summit/series_summit.

One of the major arguments in favor of SOSA and other open standards is the simplicity in hardware design, which avoids multiple ways of doing one thing. However, with reduction in the size of electronic components on unmanned platforms, comes additional complexity.

"There's the ongoing assessment of how much use is it to have the exact same hardware," says Jacob Sealander, chief architect for C5ISR [command, control, computers, communications, cyber, intelligence, surveillance, and reconnaissance] systems at Curtiss-Wright Defense Solutions (Davidson, North Carolina). "And in some cases, we're finding a lot of use to say that it's going to be the same exact hardware on all of the platforms, but for some of the smaller stuff, it doesn't make sense, which is why Curtiss-Wright has put itself in a good position to have not just the standard form-factor products that we have, but also the smaller form-factor stuff."

Put simply, the primary objective of SOSA is not to reduce size, weight, and power (SWaP). If SOSA is to eventually adopt a smaller form factor or a VITA standard, then SOSA can start playing in the SWaP-optimized SFF arena. Until then, interoperability, life cycle, and faster time to market are among the main benefits driving the adoption of open standards.

"SWaP reduction is not one of the primary principles of SOSA," says Mark Littlefield, senior manager of embedded computing solutions at Elma Electronic (Fremont, California). "However, we are seeing some technical areas where SWaP is being affected beneficially through standardization in SOSA and VITA. Power is one example. VITA 62 was significantly enhanced because of discussions and standardization efforts within SOSA, most notably the 12-volt-centric rules defined in the SOSA Technical Standard. That alone means that power supplies don't need to be over-provisioned to account for potentially different voltage needs as a system evolves over time." (Figure 1.)

Standardization and SWaP optimization on unmanned systems goes beyond the onboard electronics and extends to the control station that operates it, further complicating the role that SOSA, MOSA, FACE, and others could play in the design of these systems.

Standardizing the control station

"Control stations are important because in some cases the sensors in the unmanned vehicles are proprietary or custom and so are the control stations that control them," Hosking says. "By moving to common open standards in the vehicles themselves, there's one step forward in that they would choose a common interface – like a protocol for sending information, control information, data, and payload information – so that the transmission from the unmanned vehicle to the control station is standardized."



FIGURE 2 | Curtiss-Wright's PacStar SAVE enclosure takes a hybrid approach allowing MOSA and SOSA based systems to coexist.

In essence, if different unmanned vehicles are in the same area and use the same open standards, they could then be handled by the same control station. This level of optimized information-gathering and sharing could revolutionize the way that the military processes the momentous amounts of sensor data brought in by unmanned systems. But SOSA doesn't quite cover all the bases yet.

"I think MOSA is a better topic when considering a common control station if you look at the diversity of unmanned platforms," says Dominic Perez, chief technology officer for Curtiss-Wright Defense Solutions (Davidson, N.C.). "A SOSA small-form-factor system is still of a certain size, and unmanned systems can be far smaller than that. When we look at open standards for having commonality, it comes back to the communications and software portion of the stack. SOSA doesn't do a whole lot to define how software operates. There's a little bit there, but not a whole lot." (Figure 2.)

Some common-ground control stations may even be designed as tablets, a simple technology that may find its way into SOSA. But for now, standardizing on communications protocols and waveforms will more likely enable a single control station to speak to many different unmanned platforms.

"I also see the ground station as being a troop-transport vehicle, as being a temporary outpost, or even being a more permanent outpost," Perez says. "These same sensors that are going to deploy forward of a foot soldier are going to be

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FIGURE 3 | Mercury Systems' SCFE 6931 Dual Versal AI Core FPGA processing board is SOSA aligned and features the Xilinx ACAP Versal device that performs AI, ML, and FPGA functions.

like the ones that are forward of a soldier in an MRZR [tactical vehicle], and it's the same cluster of unmanned systems that are going to be out from your forward operating base. That's where you look for commonality in the ground system, and SOSA may play a great part in that ground station when its vehicle-based, but it's probably not appropriate when its soldier-carried or when it's a larger forward operating base. There's no need, in my mind, for SOSA style equipment in a fixed location."

The focus then turns toward reaching the maximum amount of processing that can be achieved at the edge, on the platform, directly at the sensor level. Officials claim that this will require access to connectivity, plenty of bandwidth, and optical interfaces aligned to open standards.

Standardizing edge processing

"When you look at the battlefield, I have heard a number of high-ranking officials talk about what they need more of is almost always more ISR," says Jacob Sealander, chief architect for C5ISR systems at Curtiss-Wright Defense Solutions (Davidson, North Carolina). "They need to better understand what's going on ahead of them. What comes with that – especially as sensors improve, as there's more connection points in the network, more people who want data to be shared – the big thing is the network itself. Can the network keep up with the vehicles that are a part of it? And what we would call edge computing."

This, in turn, has spurred a corresponding desire to drive commonality at a functional level. This drive extends to the kind of software being hosted, the kinds

of algorithms being used, and ensuring that open standards are being maintained in terms of communications systems.

"The modularity can be important for the hardware, but the open standards in terms of communication is critical," Perez says. "Since we have this proliferation of sensors, it is important that we think about the data that is coming out of sensors. In an uncontrolled environment, the data that is coming in is completely unstructured. I think that's where onboard processing can help to either fully structure or at least semi-structure that data before it is passed off the unmanned vehicle."

It's a fact that flexibility is key to performing the preprocessing as close to the antenna, or the sensor, as possible, which enables the unmanned sensor payload to then send the most essential data to the control station as structured, actionable information. This process can be further streamlined using artificial intelligence (AI).

CONSIDERING THE BENEFITS THAT OPEN STANDARDS BRING TO UNMANNED SYSTEMS AND SENSOR PROCESSING, THE EFFECT THAT STANDARDIZATION IS PROJECTED TO HAVE ON ENABLING JOINT-DOMAIN OPERATIONS ISN'T LOST ON ELECTRONICS MANUFACTURERS.

"SOSA is now embracing the OpenVPX 3U form factors, and those products are getting smarter and more capable because of new technology," Hosking says. "There is new FPGA [field-programmable gate array] technology, new AI technology, and machine-learning FPGAs recently introduced by Xilinx called ACAPs [adaptive compute acceleration platforms], which will be useful at allowing developers to throw different types of compute engines at the same signals to try and pick the best engine to do the best job at extracting information out of a particular signal." (Figure 3.)

Considering the benefits that open standards bring to unmanned systems and sensor processing, the effect that standardization is projected to have on enabling joint-domain operations isn't lost on electronics manufacturers.

Standardizing the joint domain

"Making these systems easier to integrate through COTS [commercial off-the-shelf] commonality and software reuse and replacement, the SOSA Technical Standard, and other open architecture standards will free up money and resources to create new capabilities," Littlefield says. "The common architecture will also make it easier to integrate multiple capabilities into a single sensor platform, like radar, communications, EW [electronic warfare], or SIGINT [signals intelligence]."

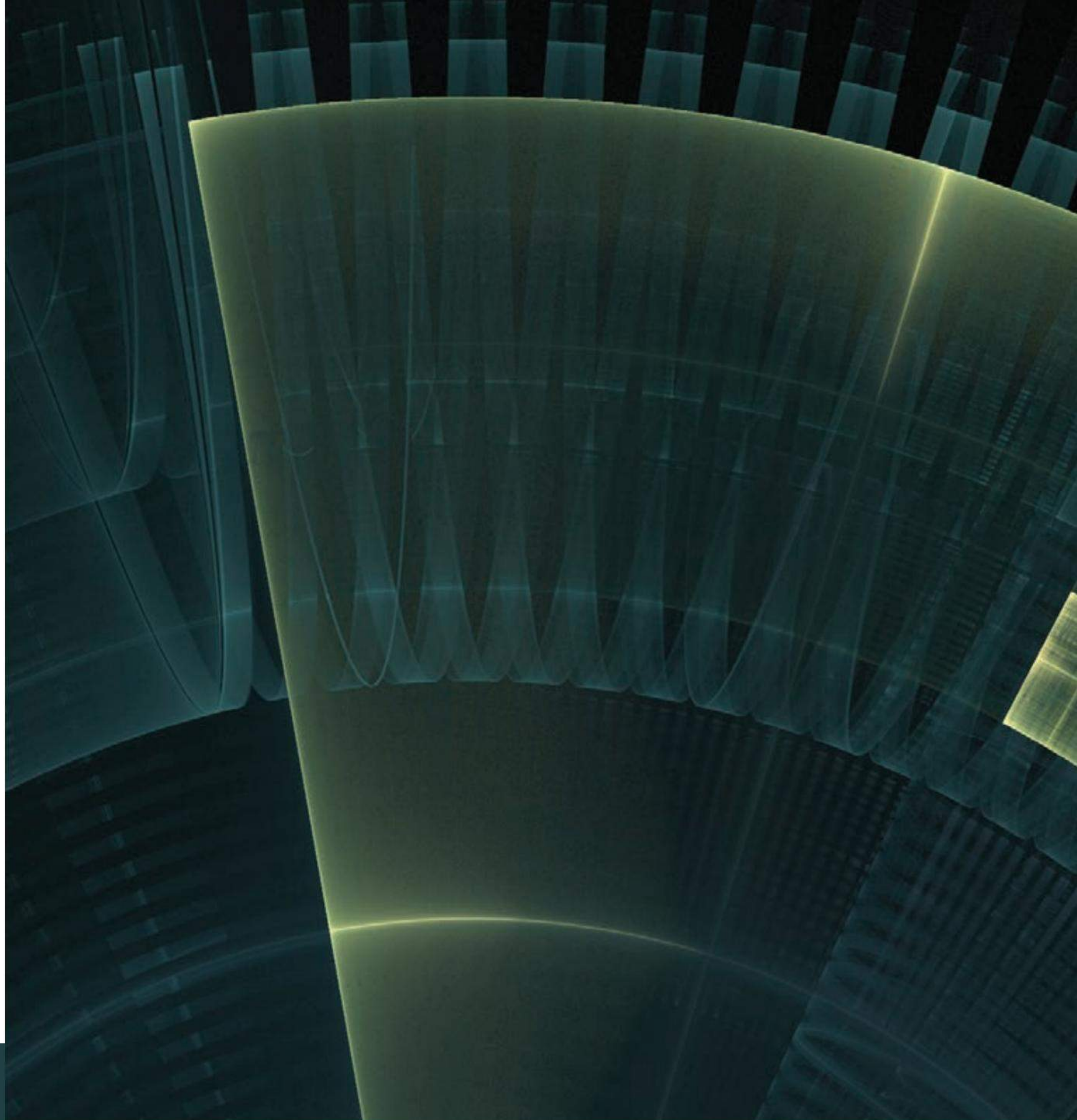
Littlefield says that this fusion of capabilities and information sources is expected to have a significant impact on the intelligence and situational awareness available to the warfighter, which will be a defining aspect of joint-domain initiatives.

Curtiss-Wright's Sealander agrees: "When all the different branches of government really embrace SOSA at the max level, you can start to see the possibility of an SDR [software-defined radio] that's used in a ground combat vehicle be used in a helicopter and be used in a fast jet when the capability, the performance, the way things are maintained are all the same.

"How we get to places like that, specifically from an unmanned platform, is if the different branches of government embrace this standardized approach at the core of it," Sealander continues. "Then you can easily see where these different unmanned solutions can have the same way of talking out to the network, and now you have this incredibly powerful battlefield to exchange data." ■

Leveraging the Sensor Open Systems Architecture (SOSA) for radar applications

By Nicholas Borton



With last year's release of Version 1.0 of The Open Group's Sensor Open Systems Architecture (SOSA) Technical Standard, more Requests for Information and contracts are specifically citing SOSA. The SOSA Technical Standard is targeting five sensor modalities: electro-optical/infrared (EO/IR), electronic warfare (EW), radar, and signals intelligence (SIGINT). What does the first version of the SOSA Technical Standard have to offer a system designer? Specifically, how can SOSA be applied to radar systems?

Radars are critical tools to armed forces for situational awareness. Potential uses include a unmanned aerial system (UAS) carrying a synthetic aperture radar (SAR), surveillance on a vessel at sea, or precision target acquisition.

As the various threats and needs of the warfighter keep increasing, so does the need to develop ever more advanced radars with an increasing list of capabilities. The Modular Open Systems Approach (MOSA) for system development provides a path to get warfighters the equipment they need to meet these requirements. Adhering to the MOSA ecosystem enables:

- › Getting sensors to the field sooner to counter emerging threats

- › Reducing integration time and costs
- › Reaching higher technology readiness levels faster
- › Enabling competition for capabilities and technology

As the Sensor Open Systems Architecture (SOSA) standard is part of the MOSA ecosystem, there is a lot of push to develop radar systems with it. With the stringent performance requirements radars need to meet, can it be done within the bounds of a modular open architecture like SOSA? Can the MOSA benefits be capitalized on while still meeting performance needs with SOSA? In fact, SOSA can indeed enable performance while simultaneously delivering the MOSA benefits.

Basic radar with SOSA V1.0

As SOSA does not define a system per se, rather components to build a system with, one of the first questions is "How much of the system should be SOSA?" Often the answer to this is "As much as possible." Regardless of the answer, this question needs to be revisited again and again throughout the design process.

Central to the SOSA Technical Standard are the SOSA modules. Although many module interfaces are not fully standardized yet, planning for how they will manifest in the SOSA infrastructure will pay future dividends. SOSA is split into two major sections

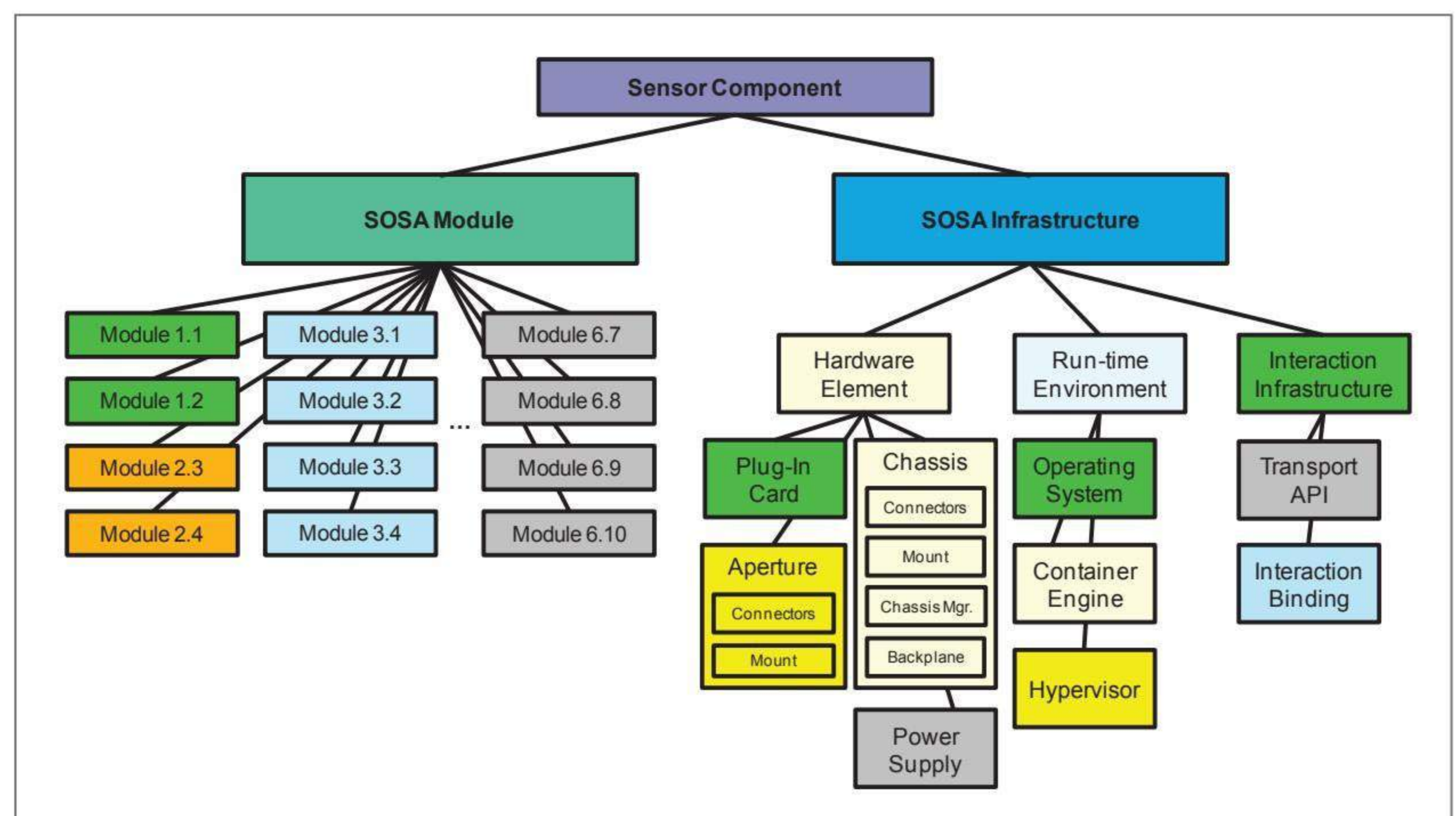


FIGURE 1 | The SOSA taxonomy shows the two major sections of standardization. Courtesy Technical Standard for SOSA Reference Architecture, Edition 1.0, The Open Group.

of standardization which is shown in the SOSA taxonomy in Figure 1.

Dealing with custom or non-SOSA components

When determining “how much of the system should be SOSA,” it is important to first consider which SOSA modules might eventually be used. Using module boundaries, basing where a system is or is not SOSA will help enable uses of future versions of SOSA and capitalize on the SOSA marketplace. To gain a sense of where to make that break, looking at the high-level data flow diagram from V1.0 of the Technical Standard can help. (Figure 2.)

Whether other standards are going to be used needs to be weighed when asking “how much SOSA.” Alternate standards might be needed for many reasons, most commonly when there will be reuse of a system or an existing system upgrade. These other standards might include Common Open Architecture Radar Program Specification (COARPS) and Fires Radar Open System Technologies (FROST). Depending on

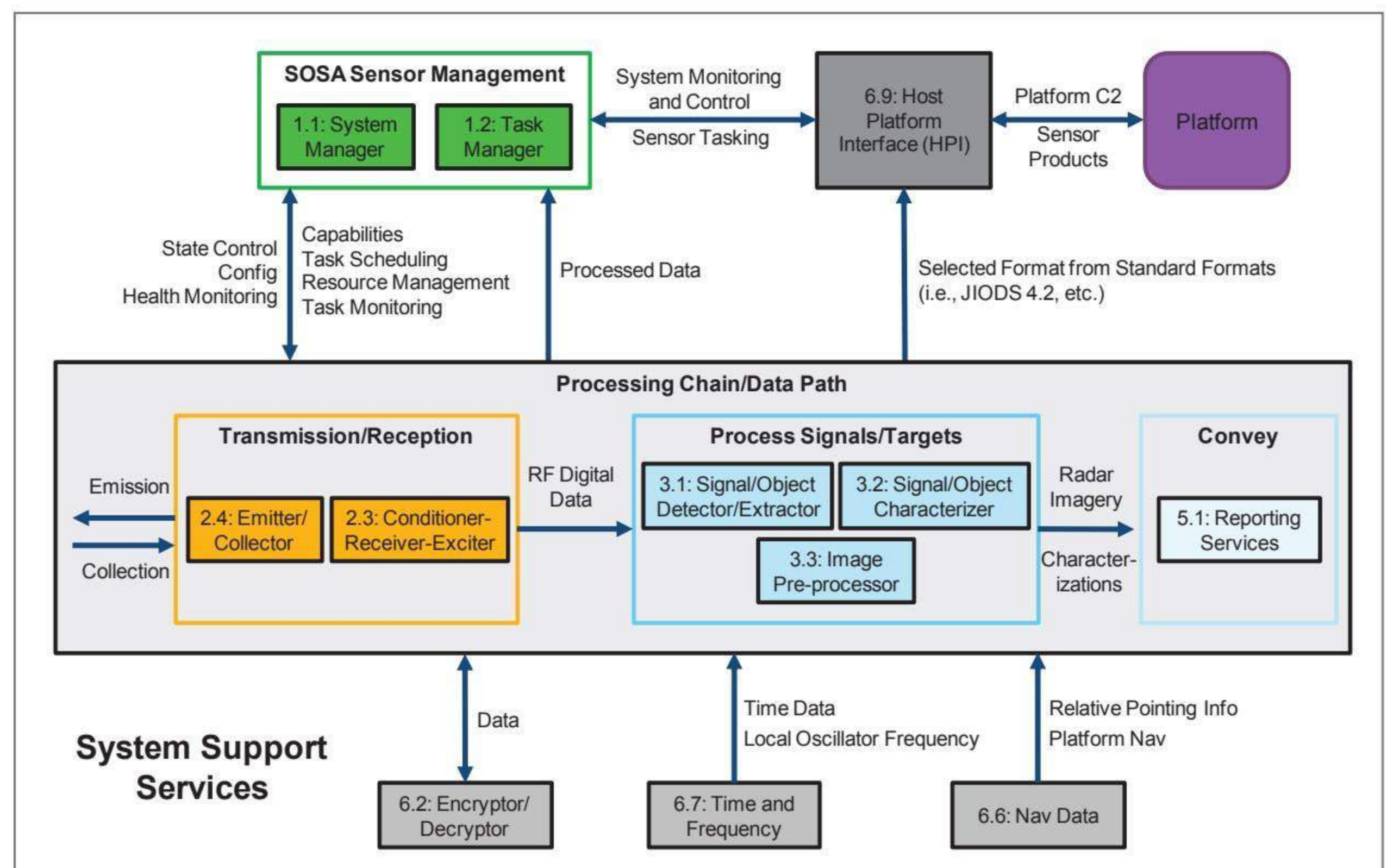


FIGURE 2 | Pictured is the high-level data flow of the SOSA Technical Standard. Courtesy Technical Standard for SOSA Reference Architecture, Edition 1.0, The Open Group.

the use case, either a clean break would need to be made between the SOSA components and the other architectures on a SOSA module boundary, or the other architectures’ components could be encapsulated inside a SOSA module’s boundaries.

As the front end of a radar provides the system with most of its mission-critical performance characteristics, it makes sense that it is most likely to be the custom portion of the sensor. From a SOSA standpoint, the front end is constrained to the 2.4 and 2.3 modules. In many radar systems, the very low-latency constraints tend to occur in the front end. Low probability of intercept (LPI) and low probability of detect (LPD) are prime examples of low-latency-inducing requirements.

Tight requirements in dwell scheduling and execution may require a large amount of hardware interconnected in a way that prevents a break between the 2.4 and 2.3 SOSA modules (depicted in Top-Level SOSA Services Context Description diagram, Figure 3, next page). If a highly custom front end is needed, maintaining the 2.3 receiver exciter module boundary and the SOSA aperture and electro-mechanical interface will enable full capitalization on SOSA for the rest of the system.

Balancing today’s needs against future functionality and technology insertions

As the designer moves past the front-end modules into the rest of the processing chain, command and control (C2), and the support modules, there is more of an ability to embrace the SOSA technical standard. Even in the case where size, weight, and power (SWaP) concerns may initially prevent SOSA adoption, adherence to the SOSA standard now will enable rapid tech insertion when new technology with a reduced SWaP becomes available.

Radar back-end processing may be demanding in terms of overall throughput, or complexity of algorithms, but it does not typically have the same real time and latency requirements of the front end. Here we are typically dealing in full dwell, or possibly scan timelines, which are much larger than the pulse to pulse (or even intra-pulse) deadlines the front end must cope with. Here the possibility of broadly embracing the Ethernet-centric SOSA inter-module infrastructure is reasonable.

SOSA design patterns are ways in which sensor functionality can be realized through SOSA infrastructure implementations. The focus on the design pattern is on the level of severability they provide, and therefore differing levels of independence from the surrounding system. The design patterns impact how functionality upgrades and technology insertions occur.

The various software patterns provide the most independence. The software patterns can be moved to any piece of hardware which is running a compliant SOSA run-time environment. That could be a SOSA PIC [programmable interface controller] with an x86 processor onboard or an FPGA SoC [field-programmable gate array system-on-chip] whose Arm cores are hosting a run-time environment.

Of the hardware patterns, either a single PIC or box-/chassis-level implementation would provide the next level of independence. In these instances, the functionality is tightly coupled to the hardware in question. To move that piece of functionality, or add new functionality in its place, the old hardware needs to be removed and new hardware which matches the backplane or mil-circular connector interfaces must be installed in its place. With the standardization which SOSA provides, finding a hardware solution already on the market is very likely.

The last major hardware pattern is the multiple PIC implementation. This is typically the most restrictive version of functionality from a reuse standpoint. With multiple PICs there are multiple interfaces to match up, but beyond just matching those interfaces, there must also be the proper interconnections between those multiple PICs. This pattern may have some common use cases such as an SBC [single board computer] paired with a GPU. Due to the popularity of the specific pattern, they might not be as restrictive as at first glance.

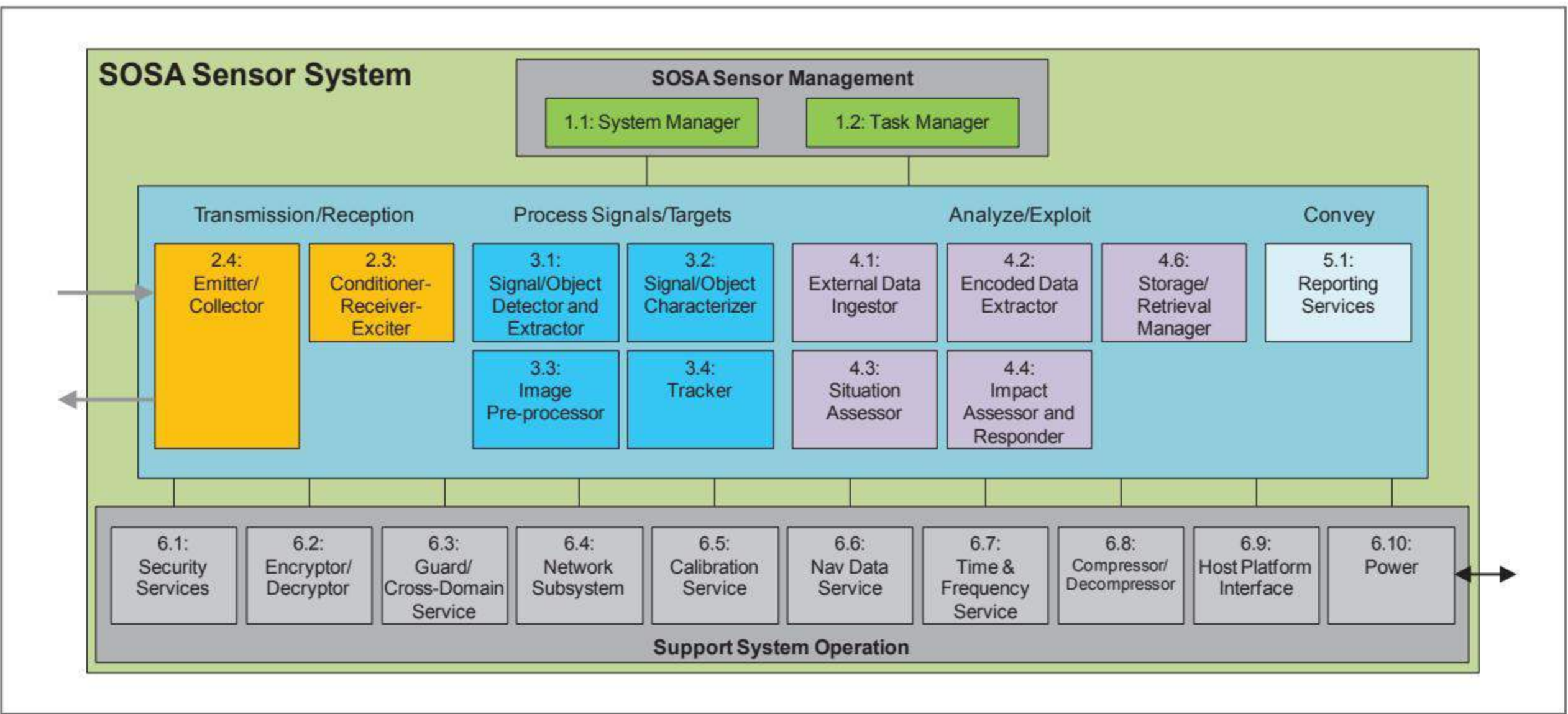


FIGURE 3 | Shown is the Top-Level SOSA Services Context Description. Courtesy Technical Standard for SOSA Reference Architecture, Edition 1.0, The Open Group.

Sustainment considerations

Strongly correlated with functionality and technology insertions are sustainment considerations.

As much as technology insertions are reliant on the SOSA interfaces to replace an old technology with a new one, these same interfaces are useful from a sustainment standpoint. The best of both worlds occurs when a planned technology insertion to keep pace with a threat also solves an obsolescence issue. To enable that best-of-both-worlds scenario, a plan needs to be in place to upgrade SOSA components in a system.

When reuse is leveraged properly, SOSA can enable merging among different supply chains as well. This can also be coupled with the rolling upgrades of SOSA components as well. When more sensor systems are reusing the same SOSA components, and team up for upgrades, the savings continue to multiply.

SOSA V1.0 provides a handful of tools based on standardized interfaces for building radars. These standardized interfaces provide many benefits to the development and sustainment of radars. It’s important to begin with the end in mind, as pre-planning for future upgrades and sustainment and making those components SOSA compatible will provide enduring threat-matched capabilities and cost savings. ■



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Why MOSA matters: How MOSA is shaping the future of unmanned systems

By Rodger Hosking



An MQ-9 Reaper sits on the flight line as the sun sets at Creech Air Force Base, Nevada, during late 2019. The Reaper provides dominant, persistent attack and reconnaissance 24/7/365. (U.S. Air Force photo by Airman 1st Class William Rio Rosado.)

Modern aerospace and defense platforms, especially in the growing field of unmanned vehicles, need more processing capability for compute-intense applications including AI, sensor processing, and fusion in avionics, that can be easily refreshed with new technology to meet new threats while keeping costs down and speeding time to market. Simplifying integration using an open architecture approach facilitates better affordability, scalability, interoperability, and sustainability across the entire military embedded ecosystem.

The pace of today's technology development means the traditional approach of custom-designed components, modules, and subsystems is too slow. By adopting a modular open systems approach (MOSA), the industry as a whole can provide standard technologies and a modular approach to system design – with the ability to be used in unmanned systems – that will deliver rapid innovation, increased vendor choice, and greater interoperability. This is accomplished by leveraging standard form factors, interfaces, and protocols to enable system engineers and designers to utilize standard building blocks to simplify integration, test, qualification, and cost.

MOSA is a technical and business strategy for designing an affordable and adaptable system based on modularity,

interoperability and scalability formally adopted in January 2019 by the U.S. Department of Defense (DoD) for “all requirements, programming and development activities for future system modifications and new start development programs to the maximum extent possible.”¹

With this collaborative initiative in place among three primary U.S. military services (Army, Navy, and Air Force), industry partners were able to follow suit. Companies' modular open-system architecture technologies are now able to align with the most adopted aerospace and defense industry standards, including The Open Group's FACE [Future Airborne Capability Environment] and SOSA [Sensor Open Systems Architecture] standards, HOST [Hardware Open Systems Technologies], CMOSS [C5ISR/EW Modular Open Suite of Standards], VICTORY [Vehicle Integration for C4ISR/EW Interoperability], and MORA [Modular Open RF Architecture] for a range of software, digital, RF, and mixed-signal processing products and subsystems. Such alignment means defense organizations can reduce program risk and build systems with reusable modules that span the entire data-processing chain from signal acquisition to information dissemination. (Figure 1.)

Create a common architecture

A common need for interoperability was recognized, so development on standards that embraced open systems architecture (OSA) principles began to meet the future



procurement needs of deployed systems for the respective military service units. In early 2017, the DoD issued a solicitation for Sensor Open System Architecture architectural research, which resulted in the SOSA Consortium, managed by The Open Group.

Major objectives of SOSA specifically include development and adoption of open systems architecture standards for C4ISR [command, control, communications, computers, intelligence, surveillance, and reconnaissance] to provide a common, multi-purpose backbone for radar, EO/IR [electro-optical/infrared], SIGINT [signals intelligence], EW [electronic warfare] and countermeasure systems. The follow-on benefits of alignment include platform affordability, rapid fielding, reconfigurability, easier insertion of new technology, extended life cycles, and repurposing of hardware/firmware/software.



FIGURE 1 | Compute-intensive applications, including such unmanned aerial systems as this MQ-9, use an open architecture approach to simplify integration for easy upgrades, lower costs, and faster time to market.

The major work product of the SOSA Technical Working Group is the SOSA Technical Standard 1.0 – which was released in September 2021 – that documents the SOSA architecture. This is a modular system structure, with tight integration within modules for encapsulating functionality and behaviors, and yet well-defined interfaces. These modules must be based on open, published standards, with consensus-based influence stakeholders directing the evolution, and a strict conformance validation process. The foundations of SOSA can be traced to OpenVPX and the defined slot profiles of this widely implemented open standard.

IN APPLICATIONS LIKE UNMANNED SYSTEMS, WHERE REAL-TIME DATA PROCESSING IS IMPERATIVE TO CRITICAL DECISION-MAKING, HAVING A CLEAR PATH FOR RAPID, COST-EFFECTIVE UPGRADES GIVES EMBEDDED DESIGNERS THE CONFIDENCE TO BUILD OPEN STANDARDS-BASED SYSTEMS FOR LONG-TERM SYSTEM SUSTAINABILITY.

Effects on unmanned military aircraft

Military aircraft avionics are traditionally a collection of subsystems, each dedicated to a particular fixed function. Each of these occupies an enclosure with well-defined dimensions, mounting points, and electrical interfaces for sensors, antennas, power supplies, and control ports. Changing the function within any subsystem is often quite limited, so that an upgrade to improve performance or capabilities usually means replacing the entire subsystem with a new one. Design of the internal electronic hardware and software is invariably proprietary to the vendor.

This causes several disadvantages: For one, new technology takes a long time to find its way into the aircraft, thus hampering its effectiveness against enemy assets. The cost of upgrades is extremely high because the whole unit must be replaced. Often each subsystem is sourced from a single supplier with limited opportunities for meaningful competition.

In contrast, SOSA enables the growth of a wider ecosystem, shifting the traditional methodology to a more collaborative environment in some significant ways:

1. The internal electronics, software and packaging must be based on open standard architectures, notably OpenVPX. Upgrading a SOSA system can mean keeping the existing subsystem, but replacing one SOSA-compliant plug-in card with another to add new device technology, higher performance levels, faster computing power, and higher signal and data bandwidths. (Figure 2.)
2. SOSA limits the number of different plug-in card types to a very small subset of OpenVPX profiles, enhancing interchangeability across vendors and function.
3. Smaller companies can participate in the SOSA vendor community to offer competitive solutions shortly after new technology components become available.

Meet future system needs with open systems

As radar technology continuously advances in a leapfrog fashion to overcome the latest countermeasures, advanced signal-processing techniques must keep pace to protect military aircraft. A critical factor in the effort is reducing the time required to make these upgrades and being able to replace a SOSA board with one that adds the new required capabilities is a major benefit in this effort. This means new technology is deployed years earlier than with the traditional scheme requiring replacement of the entire subsystem.

When developing open standards-based systems for unmanned vehicle electronics, designers must evaluate some specific application needs that are different than manned platforms. For example, the equipment must be easily controllable from the mission computer. Accomplishing this will entail a high-level application programming interface (API) using intuitive command functions and parameters that simplify operation of the equipment and interrogation of status and system health. For unmanned vehicles with onboard recorders, large storage capacities are needed, so devices like Mercury's military-grade solid-state drives help minimize downtime between missions. (Figure 3.)

Many unmanned vehicles are deployed to gather information about certain regions of interest. Real-time recorders capture wideband signals from radar and communications receivers as raw, digitized data that must be analyzed after the mission. These signals can yield vital information about which radars and radios are operational in the area, identify the type of enemy equipment, determine which countermeasure systems are operating, and decrypt encoded signals for content. Real-time recording of wideband RF signals plays a critical role in ensuring radar, SIGINT, and EW systems within unmanned aerial systems (UASs) and unmanned ground vehicles (UGVs) can keep pace with technological improvements.

Reduce program risk

A MOSA approach to system architecture maximizes technology reuse to dramatically reduce development time and cost. This reuse helps mitigate obsolescence risk while emphasizing commonality and interoperability across platforms and domains. In applications like unmanned systems, where real-time data processing is imperative to critical decision-making, having a clear path for rapid, cost-effective upgrades gives

embedded designers the confidence to build open standards-based systems for long-term system sustainability. ■



FIGURE 2 | Rear view of Model 5553 SOSA aligned module with two VITA 67.3D backplane connectors, each with 10 coaxial RF signals and 24 optical lines. Mercury photo.

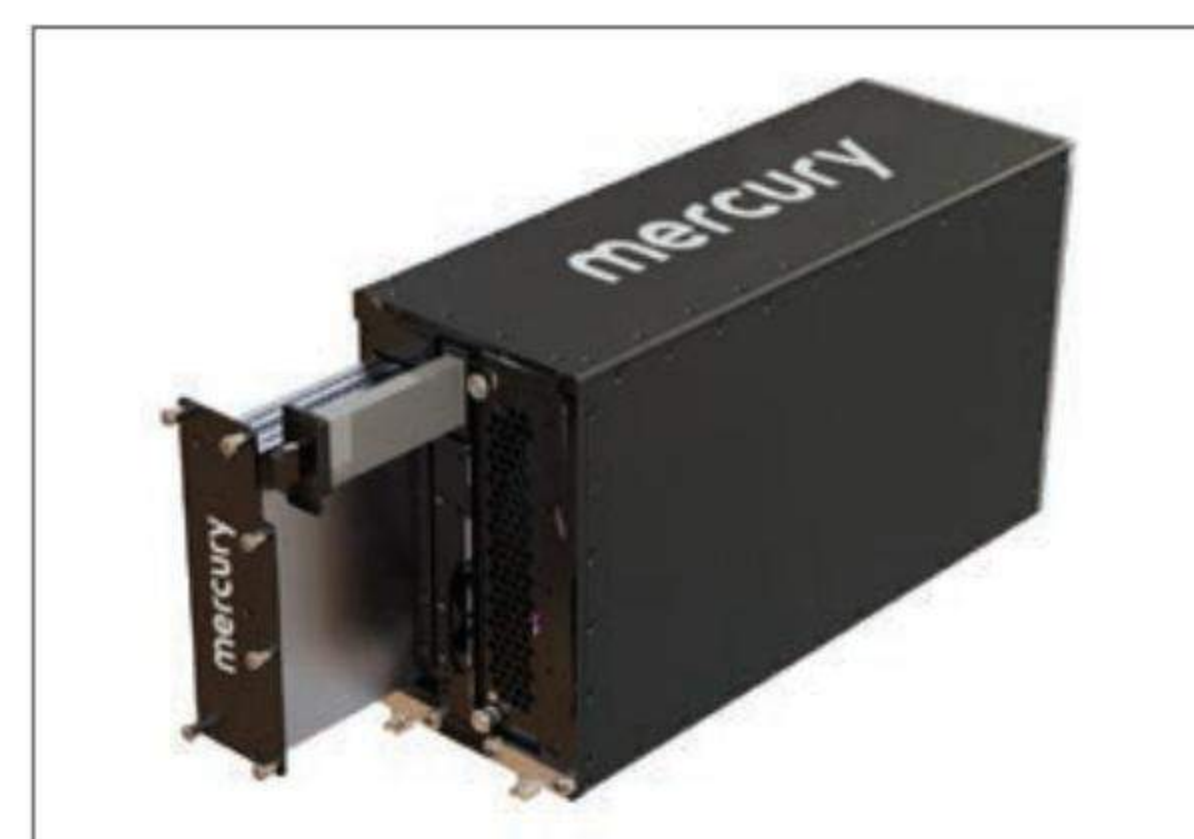


FIGURE 3 | Mercury's QuickPac drive pack holds eight SSDs (solid state drives) and enables the quick removal of all data storage from an onboard recorder via the front panel to reduce downtime between missions. Mercury photo.



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development, and strategic alliances. Rodger has more than 30 years in the electronics industry and is one of the co-founders of Pentek; he has authored hundreds of articles about software radio and digital signal processing. Prior to his current position, he served as engineering manager at Wavetek/Rockland, and he holds patents in frequency synthesis and spectrum-analysis techniques. He holds a BS degree in physics from Allegheny College in Pennsylvania and BSEE and MSEE degrees from Columbia University in New York.

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Reference: ¹ https://www.dsp.dla.mil/Portals/26/Documents/PolicyAndGuidance/Memo-Modular_Open_Systems_Approach.pdf



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Sensor Open Systems Architecture (SOSA), unmanned vehicles, and trusted computing

By Steve Edwards



Today, with the increasing use of unmanned platforms to host intelligence, surveillance, and reconnaissance [ISR] sensor applications, system integrators need to ensure that the sensor systems and the critical data they collect and store are protected from falling into the wrong hands. By their very nature, unmanned platforms – whether airborne, on land, or at sea – pose more complex problems for security. All systems, regardless if deployed on manned or unmanned platforms, are now required to adhere to the Department of Defense (DoD) mandate for a Modular Open Systems Approach (MOSA). The good news for unmanned ISR system designers is that The Open Group's SOSA [Sensor Open System Architecture] Consortium recently released Technical Standard for SOSA Reference Architecture, Edition 1.0, which defines many aspects of trusted computing for sensor systems. The SOSA standard combines MOSA principles with security to enable the rapid and affordable deployment of secure sensor systems on unmanned platforms.

Within the Sensor Open System Architecture (SOSA) Technical Standard, all security requirements are open, independent of any particular vendor or implementation. The requirements are relatively high-level and meant to facilitate the understanding of what is needed, not meant as a "how-to" regarding implementation. They operate within the framework of the SOSA software and hardware components within the technical standards, so that they mesh with the other aspects of those standards. Efforts were focused on leveraging as much of the existing capability and existing standards as possible. For

example, existing standardized security capabilities such as SYSLOG and TLS are used where applicable, rather than developing something unique for the SOSA Technical Standard. Leveraging existing capabilities, where possible, reduces cost and time to deployment.

Security within the SOSA Technical Standard is designed to be flexible: Every system is different and has different security requirements. The security capabilities in the SOSA Technical Standard can be thought of as a library of functions, to be used as needed to address security. This mindset enables

each system to tailor security to address their requirements— as security – like the rest of the SOSA Technical Standard, is adaptable. As new threats emerge and certain mitigations become less secure over time, adjustments will have to be made, a reality that will be reflected in future versions of the standard.

SOSA Service View 1 (Figure 1) documents the SOSA modules and their top-level relationships to one another. Security components defined in SOSA Technical Standard 1.0 include 6.1 Security Services and 6.2 Security Encryptor/Decryptor.

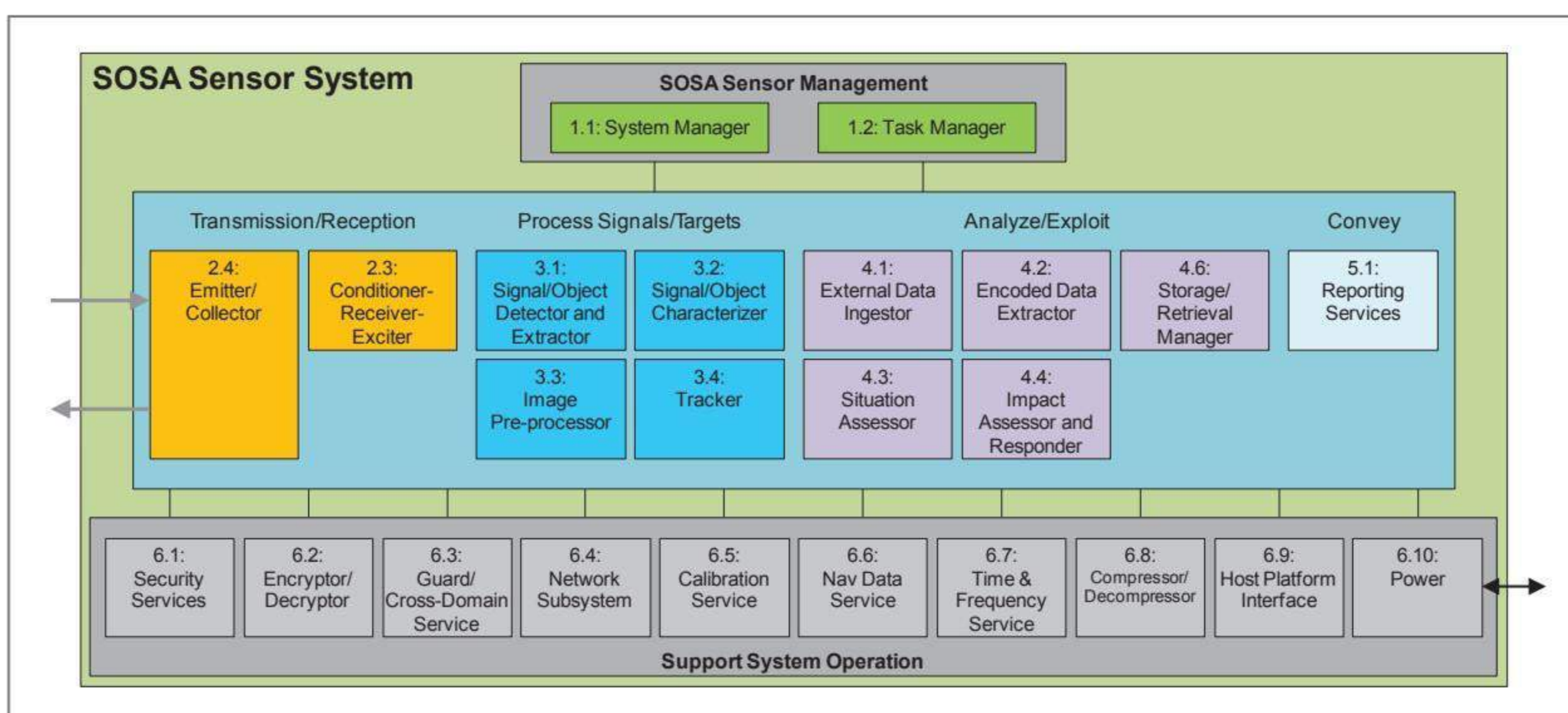


FIGURE 1 | SOSA Service View 1 documents the SOSA modules and their top-level relationships.

There is also a placeholder for 6.3 Guard/Cross-Domain Service, which will be addressed in a future version of the standard.

SOSA security services

SOSA Security Services contain a set of functions that provide a standardized way of ensuring the integrity of the system. It is a toolbox to be used to address the security requirements within a system.

For example, the SOSA Technical Standard includes functions that monitor and assess the integrity of the system throughout the operation of that system. At startup, the integrity of hardware and software is established, and continually monitored during operation so that changes are flagged and handled accordingly. When a system starts up, security evaluates the integrity of that system and determines it to be protected, degraded, or compromised. The integrity of the system is okay in a protection state. If there is an issue with integrity of some components, then the system is considered degraded or compromised depending on how severe the issues are. In this case, it is up to the system to determine what to do. It may continue to run in a less secure state, prohibit certain modules from running, or even shut down.

There may be security requirements outside of the standard that are not covered in the SOSA Technical Standard, and that is fine. In that case, the requirements are not implemented within the framework of the SOSA Technical Standard, but if SOSA does cover the mandated security components that are required, and the program will make use of them, then they must be implemented in accordance with the requirements specified in the technical standard. So, if your system is going to use TLS or SYSLOG, for example, they are covered by other standards, but if startup is going to be performed securely, the SOSA Technical Standard defines what is required for implementing it.

Security services in the SOSA Technical Standard 1.0

Secure startup: Monitor/assess the integrity of the system during initialization and continuing through operation.

Audit: Audit logging/processing of system events.

Authentication: Verifies that a module (generally – but not always – in SOSA, “module” refers to a software module) instance is intended to be used on the system.

Authorization: Grants access to privileged functions within the sensor.

Data at rest and data in transit (Data in motion): Ensures confidentiality, integrity, and availability of data stored within nonvolatile memory or transiting on a SOSA system.

Encryptor/decryptor: Provides cryptographic functions both for DAR for confidentiality, integrity, availability of system.

Intermodule interaction: For data in transit, provides confidentiality, integrity, and availability to data traversing between modules (leverages TLS/DTLS). At this time, only data traveling between modules within a specific system are covered by the SOSA Technical Standard.

Key management: Provides a mechanism for loading, storing, retrieving, and managing SOSA controlled keys within a system. SOSA key management doesn’t define how to control every one of the many keys in a system, many of which might be used outside of the SOSA key management. For example, it doesn’t define those keys used to start up an individual plug-in card, or keys used for TLS, which makes use of session keys. Those types of keys are created as needed and destroyed when the session ends. They are controlled within the TLS domain, for example, not by the SOSA key management.

Software package verification: Assists the runtime environment with verification of software packages to authenticate their use.

Zeroization: Provides a mechanism to remove/erase critical security parameters (CSPs) such as keys, passwords, and certificates.

System security life cycle

Holistic security is multidisciplinary and is needed throughout the system life cycle, which starts with design and runs through build, test, operate, and maintain before ending at retire. (This process might refer to the entire system life cycle.) Within the SOSA Technical Standard, for security the focus is on runtime, the operational and maintenance components of the system life cycle, which begins at startup and proceeds from runtime to shutdown and ends at the maintain phase.

Runtime security

Ensuring runtime security involves continual monitoring of security states. The startup states continue to work and monitor the system to understand any changes in status that might affect integrity. There is a standardized set of services that can be used to provide data integrity (for data at rest, data in transit, and key management), detection of anomalous behavior for things like SYSLOG, and – in the case that anomalous behavior is detected – being able to respond to it by zeroizing critical security parameters.

The SOSA Technical Standard does not currently contain any content that defines secure shutdown, but discussions are underway and it's expected that the subject will be covered in future versions of the standard.

Interoperability

Interoperability enables disparate systems to exchange data and information and work together. It's achieved at the interface between modules by having well-defined interactions and behaviors between modules. Within the SOSA Technical Standard there are different hardware modules – for example plug-in cards (PICs) and software modules – that may be created by different vendors.

It's important to make sure that these various elements can work together correctly. In many cases, they will have security aspects and will need to be authenticated (and perhaps authorized to use privileged functions) and they will also need to be able to send data back and forth between the modules. There is an entire group within the SOSA Consortium, called Inter-Module Interaction, that works on defining those APIs [application programming interfaces] and what the parameters that get passed back and forth are, to ensure that at the interaction level (the API level), there is common set of functions and data that gets passed back and forth so that the modules can communicate. That also applies, off-sensor, to other systems on a platform going forward.

Within the SOSA Technical Standard, the Security Services group works with the Inter-Module Interaction and Data Modeling groups to make sure that the parameters needed to ensure security are defined so that modules making use of security services can do so in a standardized way, and can interoperate with those security services and with each other.

Security and plug-in cards

Generally speaking, the internals of the various PICs and how they deal with security is the purview of the vendor, which means that the security requirements of the SOSA Technical Standard apply at the interface of the PIC. For example, SOSA does not directly impose internal requirements on how a particular PIC will boot securely. However, security requirements do apply to modules that will run on the PIC, and certain functions, such as secure startup, will want to know the integrity of the PIC. Functions will want to know how to verify that the PIC is who it says it is and will want to know what information the PIC will provide to inform that it has started up in a known secure state. That means there will need to be information passed back and forth.

Modules running on the PIC can use security services for the various security-related functions, and then communicate between where those security services are located (on a PIC in the system, most likely). The ability to communicate must be provided, typically via Ethernet, so that security services can gain the information needed to run and perform its functions.

To make the implementation of security on a PIC easier, the system designer can use a trusted platform module (TPM, an international standard for a secure cryptoprocessor), FPGA [field-programmable gate array], and root of trust. TPMs are used for encryption, storing certificates, and hardware attestation support, all of which

are useful from a security context in the SOSA Technical Standard. For Intel-based PICs, having a TPM onboard is now standard practice. TPMs can be implemented as dedicated pieces of hardware. If an FPGA is available on the PIC, there are software TPMs that can be used. Hardware cryptography can also be used within the FPGA to handle some of the TPM functions. Root of trust, which is a generally trusted entity on the PIC, can be implemented in hardware, which is more secure, or in some cases can be implemented in software. Root of trust is discussed within the current SOSA Technical Standard but is not yet defined.

SOSA Security Services does not address every cryptographic key, password, or certificate in the system. Also, the internal bring-up and integrity of a PIC is not covered by security services today. At the system-to-system level, SOSA Security Services does not currently address security between SOSA systems on a platform, or between a SOSA and a non-SOSA system. SOSA does contain the concept of a "host platform interface," which is likely to be used in the future for defining secure intersystem communications. **MES**



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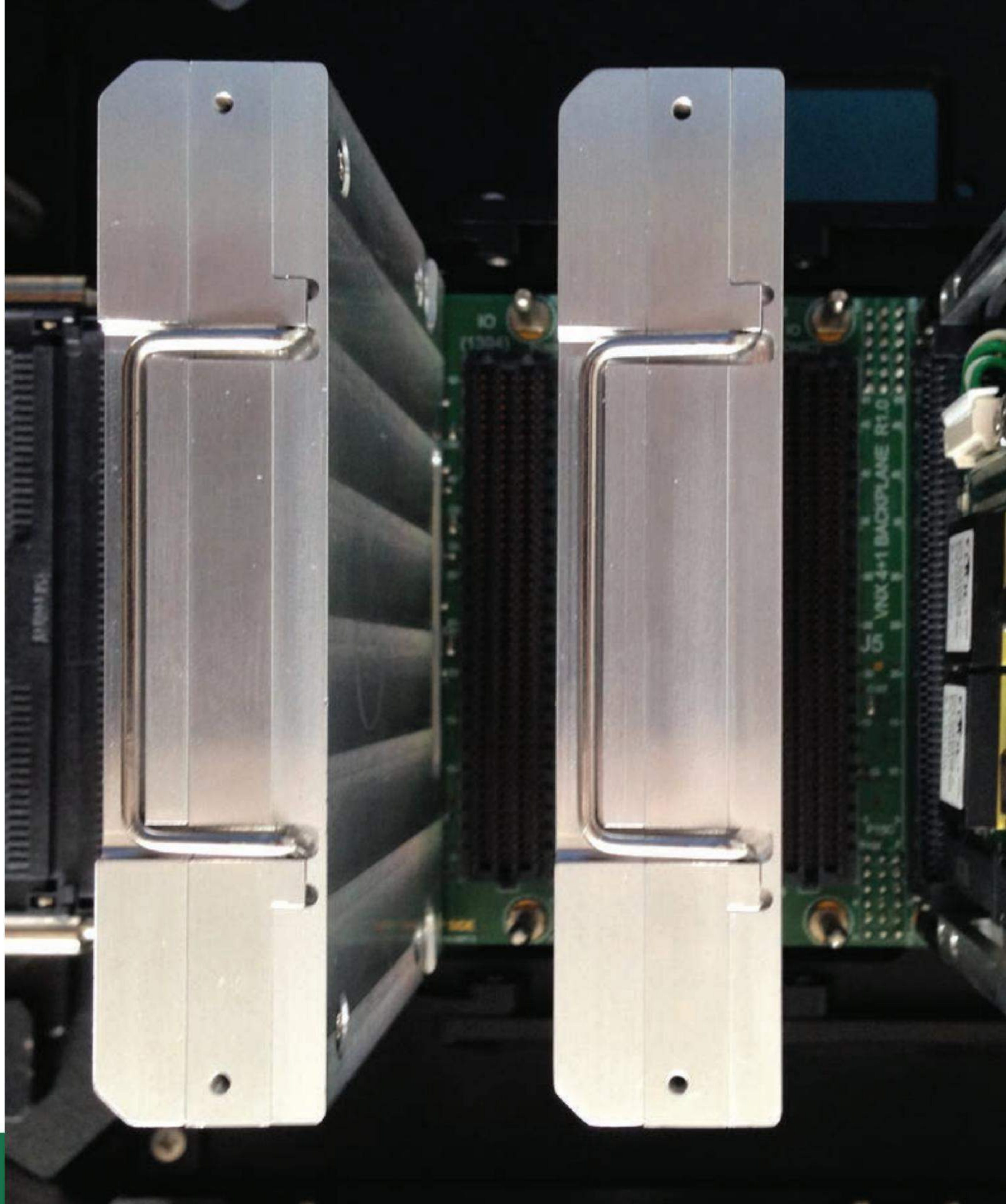


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Introducing VITA 90, the latest rugged small-form-factor module standard

By Bill Ripley, Andy Walker, and Mehmet Adalier



VITA 90 is a new small-form-factor (SFF) standard that is a direct descendant of VITA 74, an inherently rugged module standard with a compelling size, weight, power, and cost (SWaP-C) proposition, and aimed at use in many military and aerospace applications. This standard has been causing quite a ruckus within the MIL-rugged embedded systems community lately, as VITA 90 has been selected by a government-led consortium of manufacturers and integrators for inclusion in The Open Group's Sensor Open Systems Architecture (SOSA) Technical Standard, published in 2021.

The VITA 74 rugged module standard was referenced within the SOSA Technical Standard Version 1.0 – released in the fall of 2021 – and will be updated to VITA 90 in the upcoming SOSA 2.0 revision, due in late 2022. A typical VITA 74 and VITA 90 module in its simplest form is shown in Figure 1 and is approximately the size of a deck of ordinary playing cards. Both standards have an electronic architecture similar to VITA 65 OpenVPX. For the last two years, there has been a lot of work done behind the scenes to transform VITA 74 into VITA 90 to meet the technical attributes of SOSA.

Design considerations for VITA 74.0, VNX

Going back in time, the technology behind this small-form-factor (SFF) standard was initially developed by engineers at Themis Computer. Building on the successful performance of the VITA 57.1 FMC standard, engineers at Themis chose to use the Samtec high-speed, high-density SEARAY connector as its primary module-to-backplane interface, as well as the interface between the backplane and the front panel I/O transition board (IOTB). The right-angle female SEARAY connector was selected to be used on the module, with the corresponding straight male SEARAY connector selected for the backplane. This original NanoATR design defined two module sizes: a 19 mm module using the 400-pin SEARAY, and a 12.5 mm module using the 200-pin SEARAY.

The NanoATR concept was brought to the VITA Standards Organization (VSO) to be considered for a standard describing SFF computer and payload modules to be used in embedded systems targeted towards medium-sized unmanned aerial

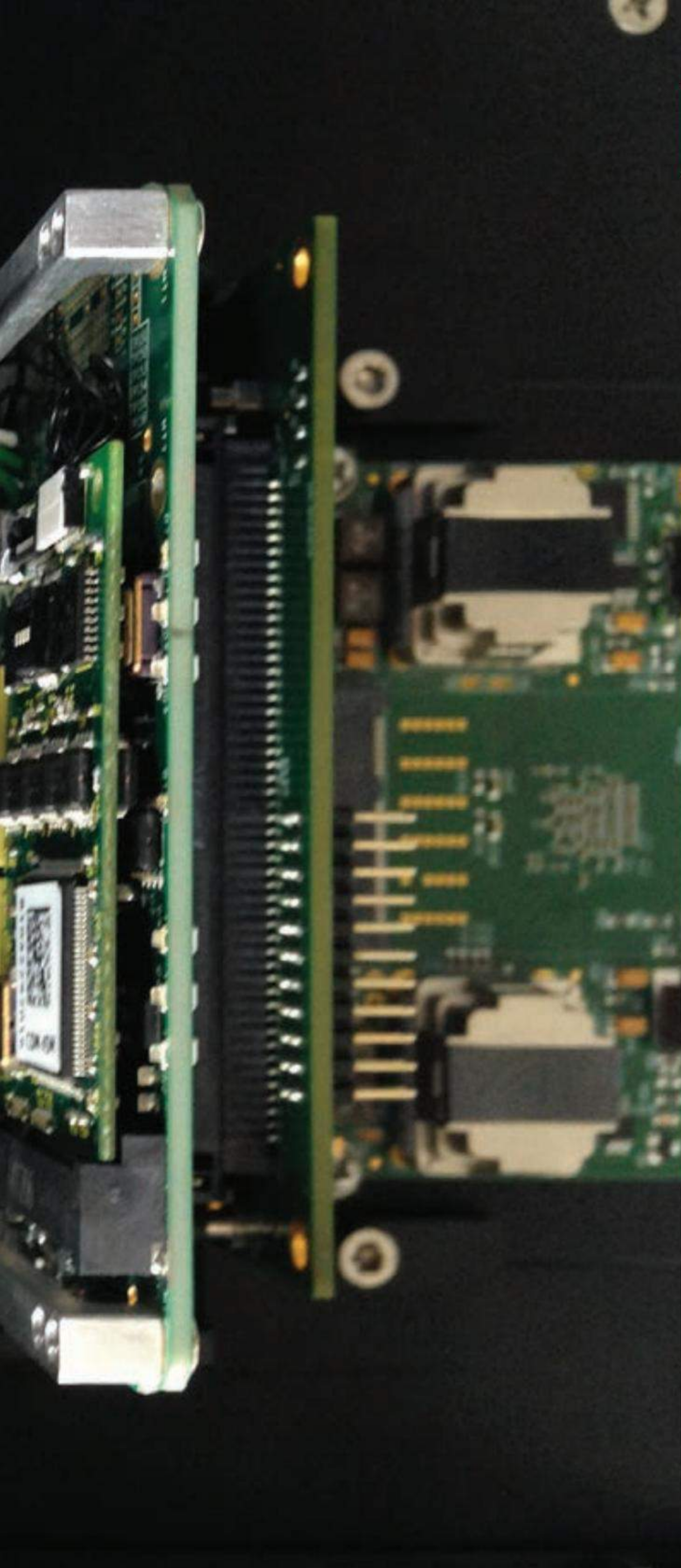


FIGURE 1 | VITA 74.0/VITA 90.0 19 mm baseline configuration module. Image courtesy Trident Infosol.



FIGURE 2 | A VITA 90 VNX+ module base card with 240-pin connector and full connector module. Samtec photo.

vehicles (UAVs) and other rugged aerospace applications. The proposal gained both traction and sponsors and became VITA 74, one of three potential SFF standards being considered at the time: VITA 73, VITA 74, and VITA 75. Of the

three standards, only VITA 74 had the backing of corporate sponsors for submission to the ANSI standards organization for ratification.

After that process was complete, VITA 74 was published as the joint ANSI/VITA 74.0-2017 standard. The standard was given the moniker VNX, a name befitting the unofficial “nano” derivative of VPX.

From its inception, VNX was never intended to replace VPX, but was instead meant to bring the essential tenets of the VPX architecture into rugged airborne, space, and ground platforms that were physically too small to accommodate a VPX system.

The ANSI/VITA 74.0-2017 base standard was released with a list of future dot-standards that will optimize complex VNX system I/O solutions for future applications. Two of these dot-standards would add the concept of backplane “Connector Modules” required to facilitate high-speed/high-bandwidth optical and coaxial RF/Video data transmission for both inter-slot and intra-system digital signaling. Another dot-standard would define options to include wedgelocks, address electromechanical considerations for single-module deployments, and define techniques for high-efficiency/high-power VNX module and system cooling. Similarly, another dot-standard defined VNX-specific power supply modules.

VITA 74.4, also known as SpaceVNX, documents specific electronic and mechanical considerations required to implement rad-hard and rad-tolerant VNX solutions in small spacecraft applications. In the process of developing these dot-standards, the VITA 74 Technical Committee reviewed the government and industry’s evolving module performance requirements and use cases; the committee decided to go all in and fully optimize the original VITA 74.0 VNX compute and I/O module’s pin assignments for maximum signal integrity, as well as implementing the OpenVPX-style utility plane, control plane, data plane, expansion plane, and I/O overlays.

Expanding VNX for high-speed fabrics and coaxial/optical signaling

The evolution of VNX from a simple module standard to a family of standards that will describe the technology required to assemble complex SFF systems has been driven by military and aerospace adopters of the ubiquitous VITA 65 OpenVPX family of standards within the VSO, SOSA, and the Hardware Open Systems Technologies (HOST) communities. As a result of evolutionary changes to the SEARAY connector pin assignments, the signal integrity of all high-speed channels has noticeably improved, and the revamped planes can now exceed the signaling requirements necessary to support PCI Express 4.0 and other modern fabrics.

As companions to the SEARAY connector, new VNX connector modules have been specifically designed and manufactured to support various combinations of high-speed signaling: fiber-optic connectivity using MT ferrules, coaxial connectivity for RF and video signals, and isolated copper contacts for applications such as providing high voltages to an RF amplifier’s power supply rails. These changes were deemed to be such a revolutionary improvement over the capabilities of the ANSI/VITA-74.0 VNX base-standard, that both VITA and SOSA leaders decided that the new capabilities should be codified in a new family of standards – ANSI/VITA 90 – which is called VNX-Plus (VNX+). (Figure 2.)

VNX+ not only includes Samtec’s 400-pin SEARAY connector as defined in the VITA 90.0 base standard, but also includes new additions necessary to support use cases such as signal processors, radio transceivers, graphics processors, network and fabric switches, and other I/O modules requiring coaxial or optical MT signaling. These applications will use the 240-pin SEARAY high-speed data connector with a full-connector module,

or the 320-pin SEARAY connector with a half-connector module as defined in the VITA 90.2 dot-standard. VITA 90.3 introduces the VNX+ energy conversion module (power supply) using a 320-pin SEARAY connector centered in a VNX+ slot, and an energy storage module (hold-up capacitor and/or battery) using a 240-pin SEARAY connector, similarly centered in a VNX+ slot.

With careful engineering of the mechanical and thermal considerations, VNX+ modules can fit in many tight spaces using conventional backplanes or microbackplanes for single-module deployments. For specific applications, additional space may be recovered by employing an equivalent cabled backplane.

Pod-mounted sensor processor deployments

Considering the tight space inside a 5-inch tube (like an AIM-9 Sidewinder-sized pod), previous systems used expensive custom hardware that was hard to upgrade as threats and requirements changed. Current thinking in the SOSA and other similar communities requires the ability to upgrade or modernize hardware to keep up with the ever-evolving threats, and that requirement drives them to specify and procure standard modules with known hardware and software interfaces. modular open systems approach (VNX+ is designed to meet those requirements.

Military integrators have discovered that the VNX+ size, weight, power, and cost (SWaP-C) attributes make the standard a natural fit for not only SFF traditionally packaged ATR-style avionics boxes, but also for pod-mounted sensor and weapon systems requiring high-performance sensor interfaces in close proximity to FPGA [field-programmable gate array] and MPSoC signal processors, computers, radios, and platform I/O available as COTS [commercial off-the-shelf]/mCOTS [military COTS]

MOSA modules with standardized electro-mechanical backplane interfaces. VNX+ is the only backplane-centric COTS MOSA standard which can be deployed as vertically oriented conduction-cooled modules on a traditional horizontal backplane, mounted longitudinally (i.e., along the long axis), within the usable area of a 5-inch diameter tube as used for an AIM-9X Sidewinder-sized sensor pod, or within a 6-inch diameter tube as used for the Coyote, as well as other similarly small payload pods or UAV fuselages. (Figure 3.)

Another SFF standard included in the OpenVPX family and SOSA 1.0 is called "Short VPX" (sVPX). sVPX is purposely designed to be the same width as a conduction-cooled 3U VPX module, with the same connector and connector module, except that the PCB area is reduced to 100 mm by 100 mm, instead of the full 3U size of 160 mm by 100 mm, but with a significantly wider slot pitch. Figure 4 shows a 6-inch Coyote-sized housing with

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a VNX module and an overlaid sVPX module, shown without the VPX back-plane and I/O connectors.

As the sVPX module is too large to fit in the available space, it can be shown that sVPX, oriented vertically as shown, is best suited for 7.0-inch tube or non-standard applications. Similarly, the full-size 3U VPX modules are best suited for 10-inch or larger tubes when oriented the same vertical manner. However, 3U VPX modules are often efficiently mounted horizontally in systems of this size, with enough vertical space to enable stacking of the requisite number of modules.

Space use case considerations

VNX is also being designed into space applications. SpaceVNX (VITA 74.4) and SpaceVNX+ (VITA 90.5) were designed from VNX’s inception to target small sats, including 1U to 12U CubeSats, and also for space rovers for critical applications that require high levels of computing and data-transfer performance. The SpaceVNX+ in-band protocols such as SpaceFibre, SpaceWire,

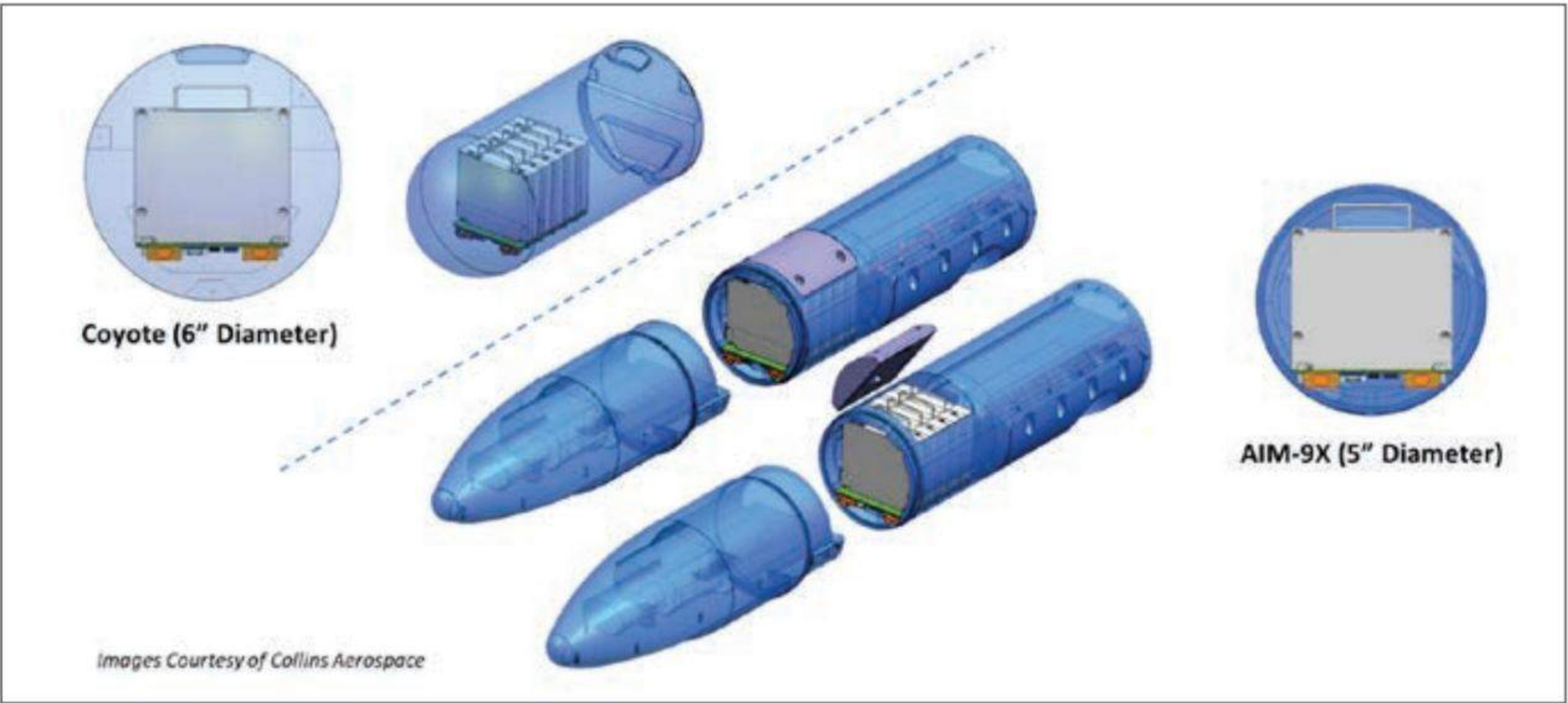


FIGURE 3 | VNX+ example system in Coyote and AIM-9X pod.

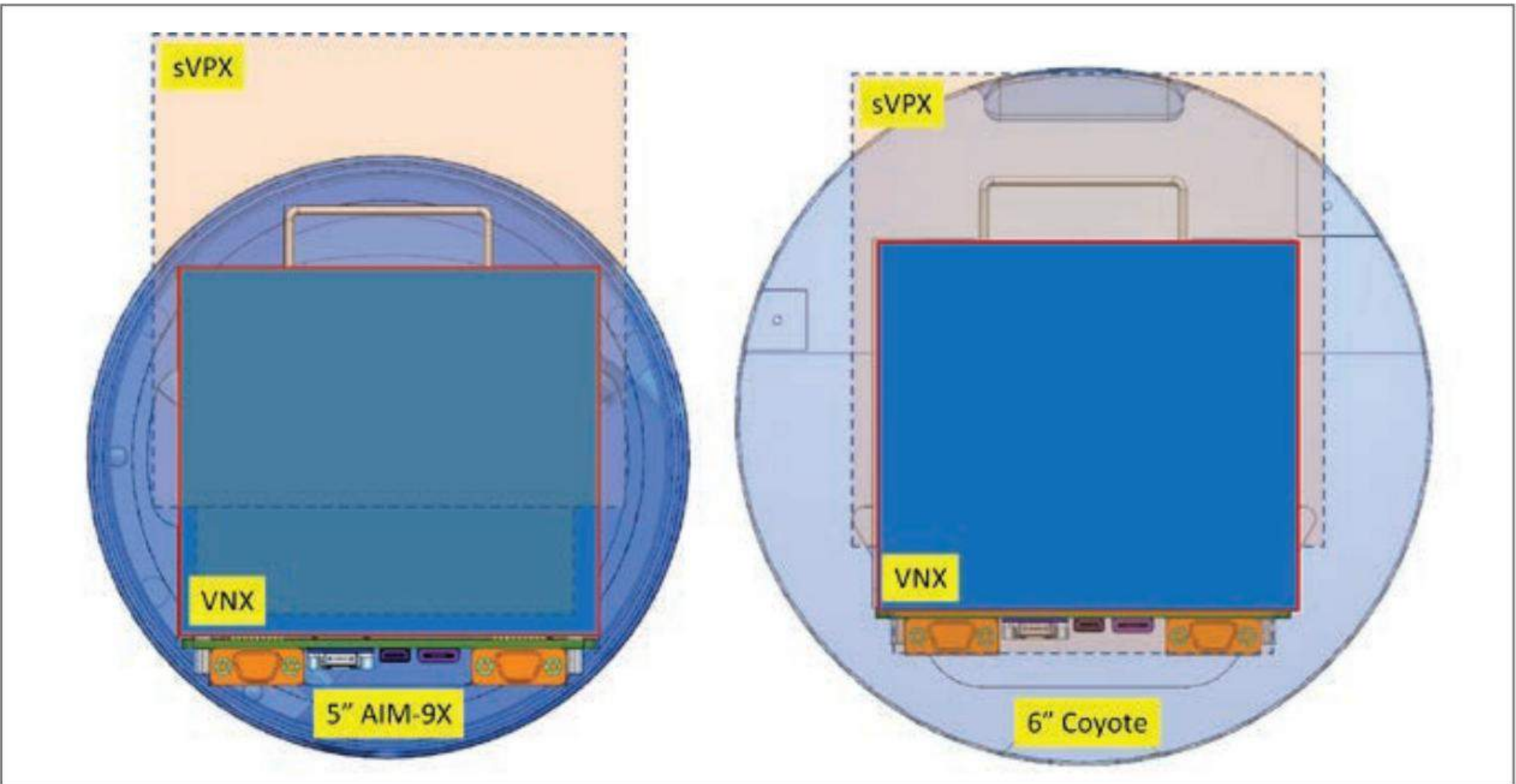


FIGURE 4 | Examples of VNX+ & sVPX modules in 5-inch and 6-inch diameter pods are shown.

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VNX+ thermal performance targets

Demands to fit in ever-tighter spaces, coupled with faster and wider data paths between sensors, signal processors, and compute modules, has made it necessary for VNX+ to support higher-power components and even denser module packaging. The power rails and grounds are enhanced in the new standard. New options include a legacy balanced 3.3 V, 5 V, and 12 V power system or a new unbalanced “12 V heavy” power system. The VNX+ energy conversion module (ECM) dot-standard is proposed to allow up to three load-sharing power modules to be used in a system, with a companion energy storage module providing input power dropout and transient protection. The integrated system must employ appropriate cooling technologies for its specified environment.

To understand the thermal limits of individual modules constructed using differing cooling strategies, studies are being conducted to define the upper power dissipation boundaries of practical VNX+ signal processing modules.

Considering the mechanical envelope studies discussed earlier, coupled with a little algebraic extrapolation, it appears that a system requiring a reasonable number of high-power SFF modules, each dissipating 60 to 80 W or more, which must be constrained in a very small package (such as a 5-inch diameter sensor pod), may now be built using a standards-based architecture employing practical advanced cooling technologies, such as oscillating heat pipes (OHP), to carry the heat away from the module to the dissipating thermal interface. Use of OHP technology should enable multiple modules to each spread their thermal load evenly across their primary thermal interfaces, with a large number of VNX+ modules oriented vertically along the long axis of a small diameter sensor pod, with the internal chassis cooled by conduction, ram air, fan forced air, or a liquid cooled heat exchanger.

High-power use cases are being verified through continued modeling and laboratory testing. Test results and use case examples showing the expanded limits of the VNX+ power dissipation envelope will be published. (Table 1.)

Many modules with functionality required for compute, signal processing, communications, and I/O are available or in work. Examples of VNX and VNX+ modules which exist today are currently evolving from existing VNX designs, or are new designs in process, include:

- › Power conversion and energy storage modules for low-, medium-, and high-power systems
- › IA compute modules with up to 11th-generation dual-core Intel Core i7 processors (formerly Tiger Lake), and current generation quad-core Intel Atom processors
- › NVIDIA GPGPU modules using the Jetson AGX Xavier GPU processor
- › FPGA modules using various SoCs and MPSoCs with Arm cores, using high-speed copper and optical backplane interfaces
- › RF transceiver modules using RFSocS as well as MPSoCs and companion transceiver
- › Rad-hard controller modules for space applications
- › I/O modules for MIL-STD-1553, ARINC 429, and MIL-1394B/AS5643 data buses
- › I/O modules with RS-232/422/485, CAN, and Gigabit Ethernet interfaces
- › Gigabit Ethernet switches with L2/L3 and 10 GbE uplink ports
- › Storage modules using mSATA SSDs
- › MEMS inertial measurement units with GPS

| VITA 90 VNX+ Module Shell Material Thermal Study | | | Aluminum | | | Copper | | | Oscillating Heat Pipe | | |
|---|---------------|-------|----------|------------|-------|---------|------------|-------|-----------------------|------------|-------|
| Power | Component | Watts | Rise °C | Ambient °C | | Rise °C | Ambient °C | | Rise °C | Ambient °C | |
| | | | | +55 C | +71 C | | +55 C | +71 C | | +55 C | +71 C |
| High 95W | FPGA | 80 | 145 | 200 | 216 | 68 | 123 | 139 | 49 | 104 | 120 |
| | Optical CODEC | 7 | 132 | 187 | 203 | 71 | 126 | 142 | 39 | 94 | 110 |
| | NVM | 5.2 | 125 | 180 | 196 | 60 | 115 | 131 | 39 | 94 | 110 |
| Med 55W | FPGA | 40 | 86 | 141 | 157 | 49 | 104 | 120 | 38 | 93 | 109 |
| | Optical CODEC | 8 | 88 | 143 | 159 | 52 | 107 | 123 | 39 | 94 | 110 |
| | NVM | 5.2 | 78 | 133 | 149 | 40 | 95 | 111 | 28 | 83 | 99 |
| Low 35W | FPGA | 20 | 63 | 118 | 134 | 40 | 95 | 111 | 32 | 87 | 103 |
| | Optical CODEC | 10 | 66 | 121 | 137 | 43 | 98 | 114 | 35 | 90 | 106 |
| | NVM | 5.2 | 55 | 110 | 126 | 30 | 85 | 101 | 22 | 77 | 93 |

| | AMB | Die |
|-----------------|------------|-----|
| Limits (High C) | Industrial | |
| FPGA | 105 | 125 |
| Optical Codec | 105 | 115 |
| NVM | 105 | 115 |

Over Temp

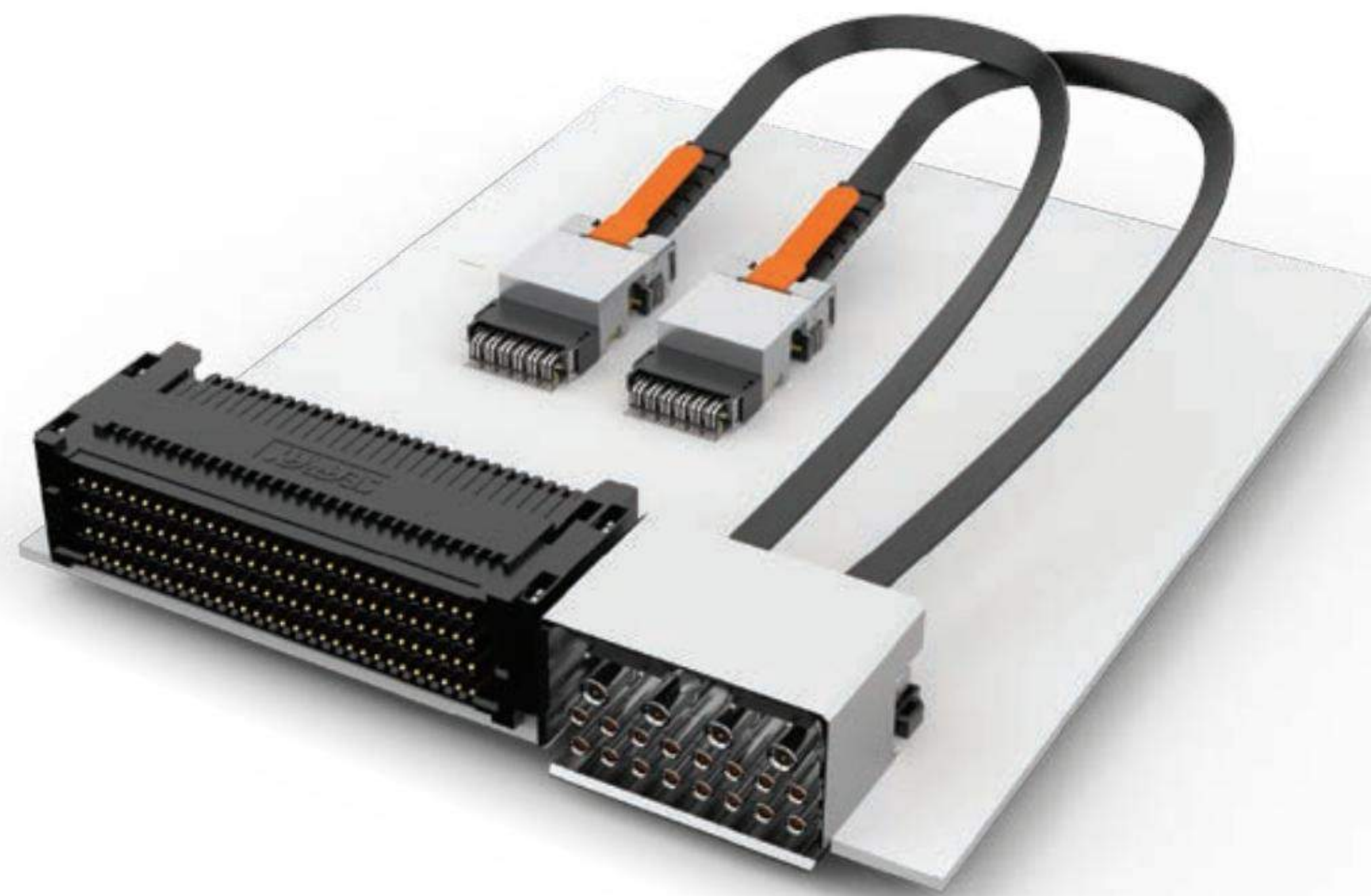
TABLE 1 | Modeled data bracketing the thermal performance of VNX modules with material variances. Note: all values are °C rise above heat sink temperature.

SOSA ALIGNED INTERCONNECT SOLUTIONS FOR SFF APPLICATIONS

VITA 90 VNX+ SOLUTIONS

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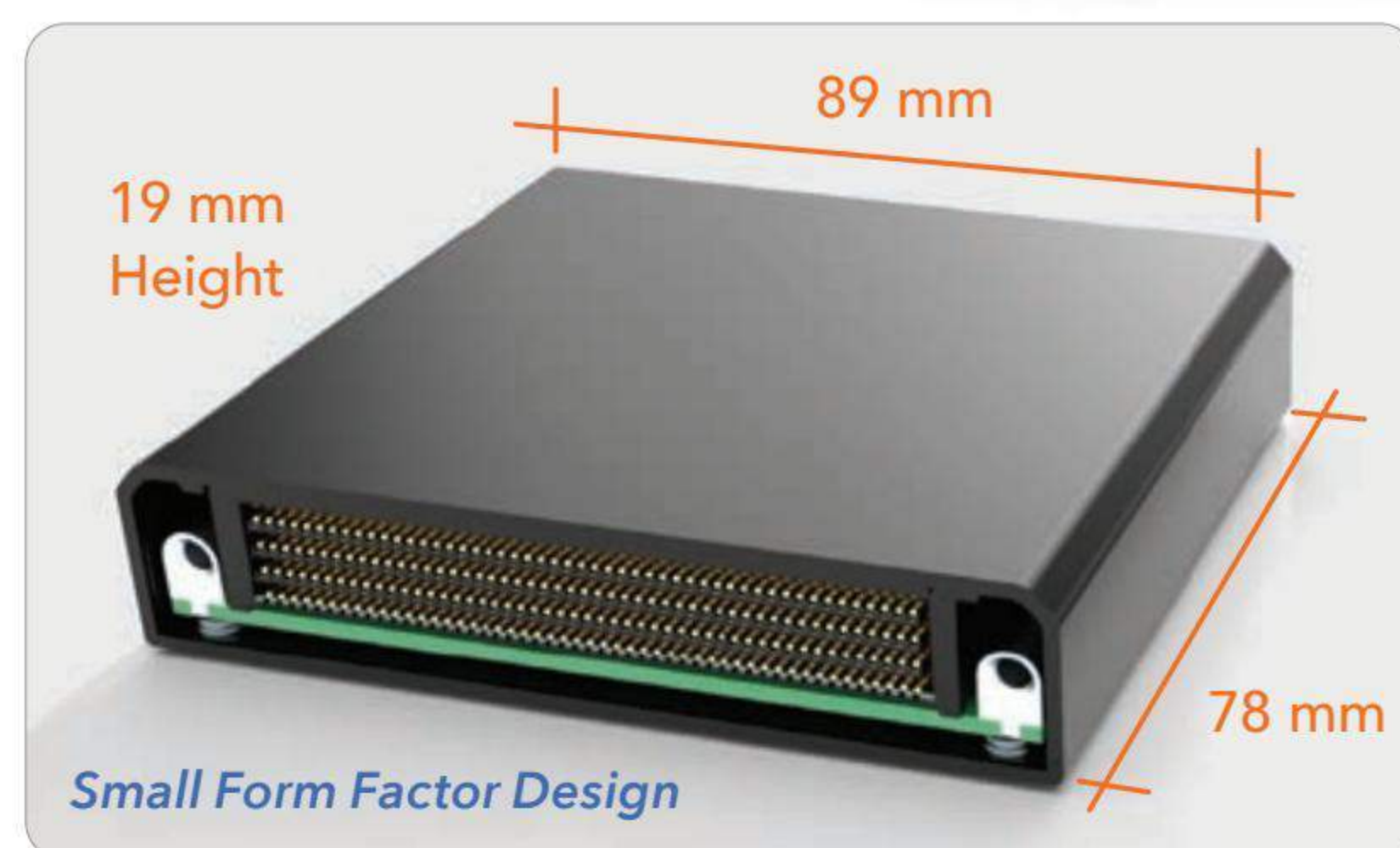


The Expanding VNX+ Ecosystem

The embedded marketplace demands SWaP-C optimized solutions. Many of these demands call for high performance but at a much reduced size and power.

VITA 90 standard-based products serve markets that require rugged performance, as well as data plane interconnect technologies that closely follow the industry's state-of-the-art.

- Small Form Factor (SFF) switched serial interconnects
- Open-frame backplane design



Application: Trident Infosol Raptor VITA 90 VNX+ COTS Computer

The Raptor is a rugged, small form factor, Commercial Off the Shelf (COTS), pre-qualified computer based on VNX standard. VNX+ is the continued evolution of the VPX standard specifically designed for significantly smaller deployments.

Featured Samtec Products:

- VITA 90 VNX+ (12.5 mm Lead-Free) 200-Pin I/O Male Connector (SEARAY™ ASP-161073-01)
- VITA 90 VNX+ (12.5 mm Lead-Free) 200-Pin I/O Female Connector (SEARAY™ Right-Angle ASP-161074-01)
- VITA 90 VNX+ (19 mm Lead-Free) 400-Pin I/O Female Connector (SEARAY™ ASP-161073-02)
- VITA 90 VNX+ (19 mm Lead-Free) 400-Pin I/O Female Connector (SEARAY™ Right-Angle ASP-161074-02)



As the military and aerospace communities move to smaller and more intelligent platforms, the requirement to build smaller systems becomes ever more important. To get more “bang for the buck,” there is an enlarging paradigm shift away from custom electronics towards COTS and mCOTS solutions. To minimize the effort required to upgrade systems through the use of common hardware, communications, and control interfaces, it is necessary to build hardware which can be conformant with MOSA standards from ANSI/VITA, SOSA, HOST, and other consortia. VNX+ is being designed and implemented with all of these requirements in mind. ■



Bill Ripley is the co-chairman of the VITA 90 VNX+ Technical Working Group and is also an engineer and business-development consultant specializing in development and sales of high-performance standards-based, small form factor, embedded computers deployed in military and aerospace rugged electronic system applications. Readers may get in touch at Bill.Ripley@Samtec.com or Bill.Ripley@Trident-SFF.com.



Andy Walker is associate director, Mission Systems Advanced Technology Center, at Collins Aerospace. His previous work ranges from devices for advanced radar systems to GaN and SiC devices for electric vehicles. His current pursuits include multifunction RF systems to provide stand-in capabilities in attritable platforms by leveraging open standards across disparately resourced platforms. Contact him at anders.walker@collins.com.



Mehmet Adalier is CEO and founder of Antara Teknik LLC. He leads the innovation and development of interoperable,

efficient, and secure communications and assured cross-domain solutions on Earth and in space. He is currently driving delay/disruption tolerant solutions for cislunar and deep-space communications utilizing SpaceVNX+. Contact the author at madalier@antarateknik.com.

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Applications for Future SOSA Conformant Solutions (archived webcast)

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Now that The Open Group's Technical Standard for the Sensor Open Systems Architecture (SOSA) Reference Architecture, Edition 1.0 has been published, products that are currently aligned to SOSA will start going through the process to become conformant to the SOSA Technical Standard. Once pronounced conformant, these products will start being designed into mission-critical applications and deployed for use by the warfighter in applications such as radar, electronic warfare, and SIGINT.

This webcast featuring industry experts covers those potential applications and the benefits – both technological and economic – that SOSA conformant solutions bring to these important missions.

Watch the webcast: <https://bit.ly/3Ayw47g>

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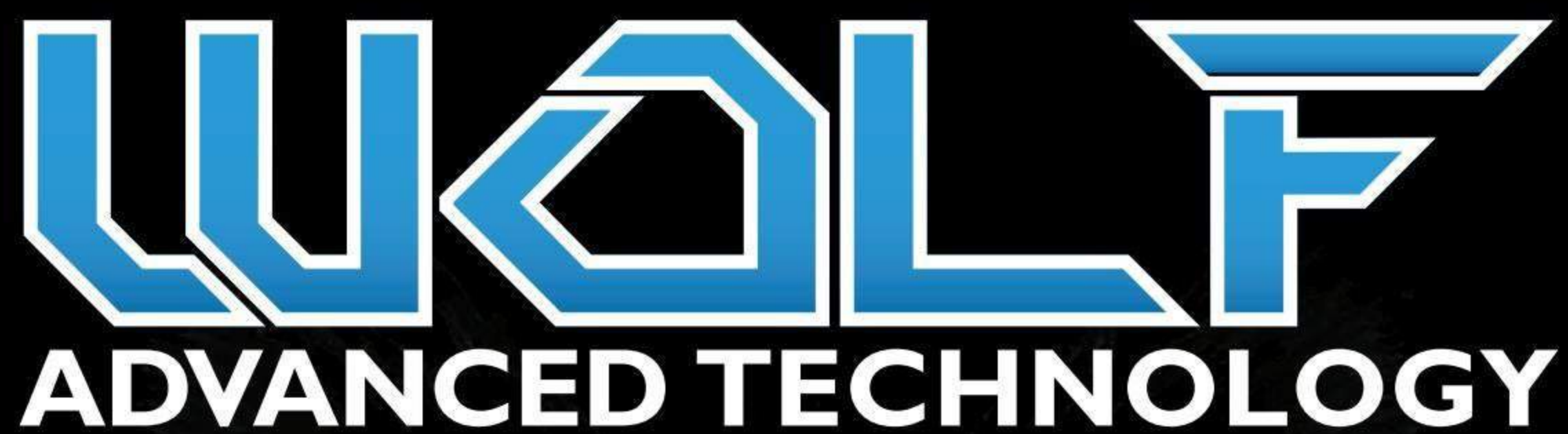
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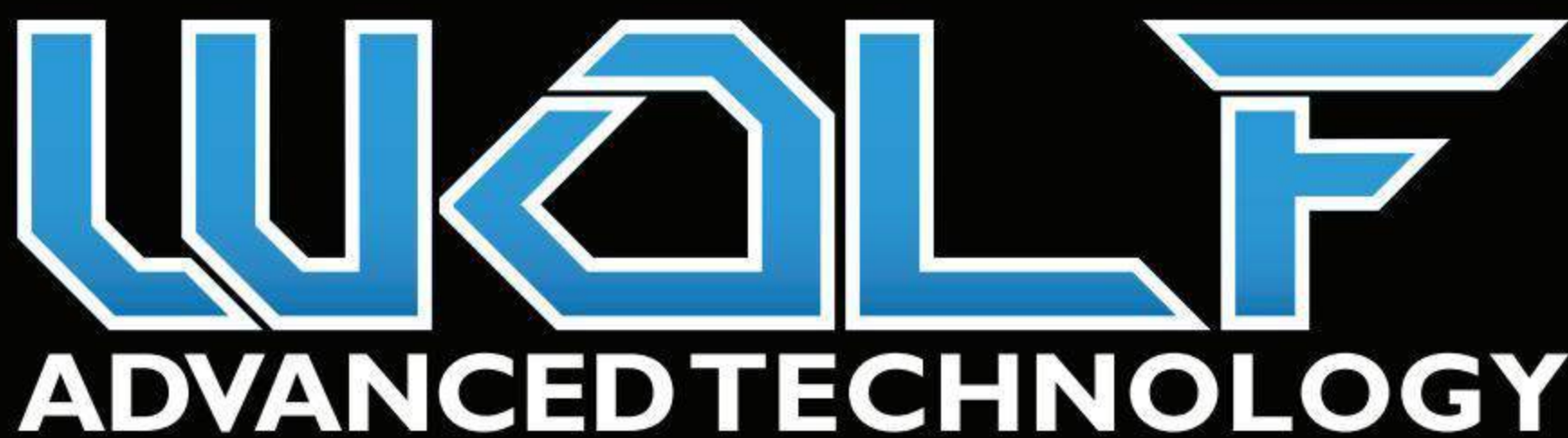
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New

**HPC with NVIDIA Ampere
& ConnectX-6**
(WOLF-144L)



- ▶ NVIDIA Ampere, 17.7 TFLOPS FP32 peak, 184 Tensor Cores, up to 100GbE
- ▶ This HPC product is ideal for data-heavy tasks such as sensor data processing and other C4ISR tasks. The embedded GPU provides advanced processing capabilities for HPC and artificial intelligence processing. The ConnectX-6 provides the Ethernet and PCIe connectivity needed to move large datasets securely and efficiently.
 - SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11
 - SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13

VPX3U-A4500E-CV

New

**NVIDIA Ampere & WOLF
FGX Converted Video**
(WOLF-1447)



- ▶ NVIDIA Ampere, 17.7 TFLOPS FP32 peak, SDI, Analog, DP, converted video
- ▶ WOLF's converted video output product includes an NVIDIA Ampere GPU which provides high performance video processing, and a WOLF FGX which provides video conversion to formats which are not native to the GPU such as SDI, analog formats, or other formats as required. The module can also be configured to be SOSA aligned with the following SOSA profiles supported:
 - SLT3-PAY-2F2U-14.2.3 Legacy Payload Slot Profile

VPX3U-ORIN-CX7-SBC

New

**SBC with NVIDIA Orin
& ConnectX-7**
(WOLF-14T0)



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- ▶ NVIDIA® Jetson AGX Orin™, 3.4 TFLOPS FP32, 200 TOPS Int8, ARM64 8-core 2.2GHz, ConnectX up to 100 GbE
- ▶ This SBC provides the data processing capability needed for HPC tasks such as sensor data processing, machine vision, and other C4ISR tasks. This autonomous module includes an NVIDIA Jetson AGX Orin, an NVIDIA ConnectX-7 SmartNIC, and a WOLF FGX which provides support for non-native video formats such as SDI and analog. This module supports SOSA aligned SBC slot profiles. The default profile is:
 - SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

VPX3U-A4500E-IO

New

**NVIDIA Ampere & WOLF
FGX SDI, Analog, Other**
(WOLF-1440)



- ▶ NVIDIA Ampere, 17.7 TFLOPS FP32 peak, WOLF FGX for capture and video conversion
- ▶ This capture, process and display product includes an NVIDIA Ampere for video and data processing and a WOLF FGX for video capture and format conversion to non-native formats such as SDI, analog, and other formats as required. The product includes a PCIe Gen4 switch, and provides support for NVIDIA GPUDirect RDMA. The module can also be configured to be SOSA aligned with the following SOSA profiles supported:
 - SLT3-PAY-2F2U-14.2.3 Legacy Payload Slot Profile

VPX6U-A4500E-DUAL-VO

New

**Display and HPC, SOSA™ Aligned and
OpenVPX Payload Profile support**
(WOLF-2448)



- ▶ Dual NVIDIA Ampere, 35 TFLOPs peak for HPC, video output support for DP, DVI, HDMI
- ▶ This dual GPU video output and HPC board includes two high performance NVIDIA Ampere GPUs and a PCIe Gen4 switch. The embedded GPUs provide advanced processing capabilities for HPC and artificial intelligence processing for tasks such as sensor data processing, machine vision, and other C4ISR tasks or C5ISR tasks. The module can be configured to be SOSA aligned with the following SOSA profiles supported:
 - Payload Slot Profiles 10.6.3 and 10.6.4
 - Legacy Payload Slot Profile

VPX6U-A4500E-DUAL-DPU3*

Advanced

**Autonomous Trusted Compute
for HPC and AI**
(WOLF-24**)



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- ▶ ** WOLF is seeking discussions with SOSA customers to finalize product configuration and features.*
- ▶ Dual NVIDIA Ampere, 35 TFLOPS FP32 peak, NVIDIA® BlueField®-3 DPU with ARM cores, Network and PCIe connectivity
- ▶ This 6U VPX includes two high performance NVIDIA Ampere GPUs and an advanced BlueField DPU-3. The DPU includes an ARM CPU with 16 Hercules A78 Arm cores, 32 lanes of PCIe Gen5, and Ethernet connectivity with up to 400 GbE. The BlueField DPU also provides the advanced security and management features required for a trusted compute node.
 - SLT6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H-10.6.4

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Standards-driven innovation: A perspective on SpaceVPX

By Tim Meade



Standards-driven product innovation creates a symbiotic relationship between systems integrators and technology developers. As new component-level technologies are introduced, they enable faster, lower-cost, and improved SpaceVPX (VITA 78.0) platform implementations. SpaceVPX systems that utilize these new technologies will have an increased adoption and deployment rate, creating improved development investment returns for the component suppliers while enabling accelerated deployment and usage of the integrated SpaceVPX systems.

In pursuit of technological excellence, microelectronics developers must continuously innovate compelling solutions that enable advancement of their target applications. Identifying and defining the best purpose-built solutions demands input from multiple sources and skillsets.

While creating truly novel technology is exhilarating and, if widely adopted, will reap proportionally large gains, it is also accompanied by numerous high-risk factors. One such risk is market acceptance and adoption rate due to the unique

nature of novel solutions. When a technology developer doesn't have a single major application upon which to focus, like an iPhone, an alternative approach is required such as targeting standards. Consider the ubiquitous nature of MIL-STD-1553, which has been deployed in nearly every military aircraft and satellite since the 1970s. Investing in MIL-STD-1553 solutions over the decades would have brought returns many times over, simply by the use and adoption rate of the technology.

Reliable and highly capable interface components based on standards like MIL-STD-1553, SpaceWire (ECSS-E-ST-50-12C), RS-485 (EIA/TIA-485), and CAN Bus (ISO 11898-x), among many others, have served generational military and space systems. Although these interface components provide a strong ecosystem of solutions supporting a multitude of systems and applications, they do not, by themselves, drive the system level interface requirements. Instead, the system architectural definition determines which components are required. Broadly adopted system definitions –



SPACEVPX (VITA 78.0) IS
A GREAT OPEN SYSTEM-LEVEL
STANDARD THAT CARRIES
INTEGRATION FLEXIBILITY,
HIGH-PERFORMANCE SIGNAL-
AND SENSOR-PROCESSING
POTENTIAL, AND EXCEPTIONAL
FAULT RESILIENCY.

preferably those which are developed and ratified through an industry standardization body – can clearly highlight opportunities to innovate component-level solutions enabling effective implementation of the open system standard.

SpaceVPX (VITA 78.0) is a great open system-level standard that carries integration flexibility, high-performance signal- and sensor-processing potential, and exceptional fault resiliency. Unit-level form factors include 3U and 6U with standard and extended length options and as many as 32 logic module slots. The standards group gave a lot of consideration toward defining the platform with no single-point failures in mind, so that redundancy is infused through the system. Yet, realizing all the promise of SpaceVPX depends heavily on the component ecosystem capable of fulfilling the demanding platform requirements including those unique to power supplies, utility modules (SpaceUM), chassis controllers, Serial RapidIO and SpaceWire switch cards, and ultimately payload cards.

High-level SpaceVPX overview

The SpaceVPX system is typified by redundant groups of slot cards, or modules. As shown in Figure 1, the module groupings fall into either the Primary (Side A) or Secondary (Side B). Within a module grouping, there are three module classes: power-supply modules, logic modules, and utility modules/SpaceUM. While the power-supply and utility modules serve very distinct roles within the SpaceVPX system, Logic modules span a range of purposes and can be refined into subgroups.

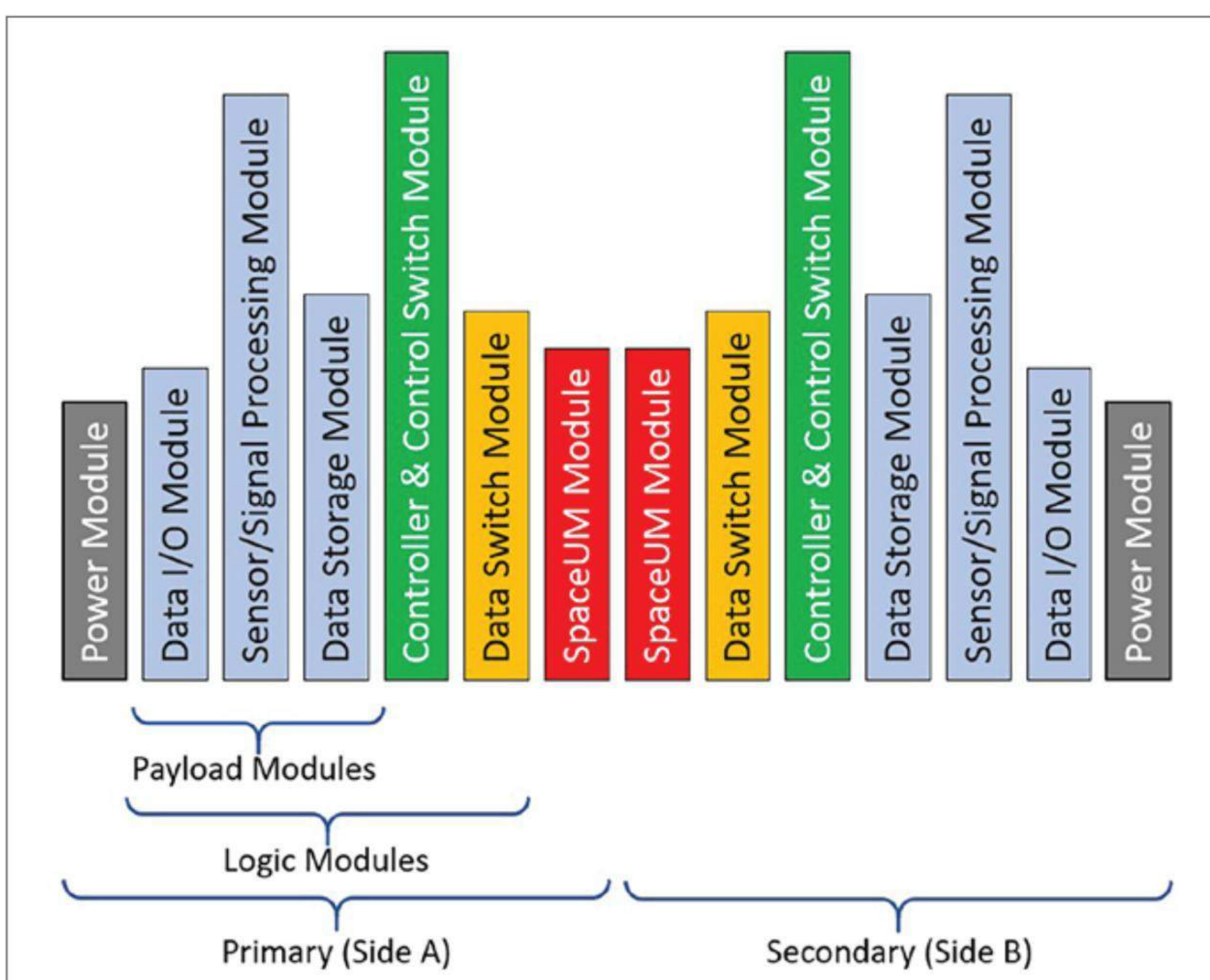


FIGURE 1 | Graph shows a SpaceVPX system high-level module overview.

Payload modules represent the slot cards that perform the system application functions and will vary widely based on the program requirements. The controller module performs chassis-management functions and communicates throughout the system on the utility plane and control plane. Finally, the data switch module provides crossbar switching of the high-bandwidth data plane communication between all payload modules.

Keeping in mind fault tolerance via redundancy is a staple of the SpaceVPX specification, cross-strapping control, utility, and data plane communication links are essential.

Interfaces and responsibilities within a SpaceVPX module

It might be helpful to further delve into the interfaces and responsibilities within each SpaceVPX module. Standing in the shoes of the module designer frequently illuminates problems where readily available component solutions are insufficient to effectively meet the system requirements. These capability gaps represent great opportunities to define and develop innovative component solutions that will enable more effective implementation of the SpaceVPX requirements. Let’s look at the power-supply and SpaceUM modules.

SpaceVPX system power-supply units (PSUs) receive external power from the satellite power bus or other specific architecture-defined voltage domain. Each power supply is responsible for generating up to seven voltage rails: +12 V/VS1, +12 V/AUX, +3.3 V/VS2, +3.3 V/AUX, +5 V/VS3, -12 V/AUX, and VBAT.

While there are not many major blocks in the power supply, the complexity is in the details, particularly when considering the limited availability of radiation-hardened (rad-hard), space-qualified, high-power-density, isolated converters capable of delivering >100 W with high efficiency. If, as is typical, the average efficiency of the 500 W supply is 85%, the module will need to thermally dissipate 75 W. That is no easy feat; especially in a 3U form factor module operating in the vacuum of space.

Advanced packaging capabilities and increasing availability of better technologies like gallium nitride (GaN) mean improved parts; further, when more rail wattage is required, the GaN converters can also be placed in parallel.

An additional untapped area of potential innovation within the power supply is integration of “smart” functions enabled through incorporation of power management bus (PMBus). PMBus provides many useful, converter-oriented, functions capable of dynamically adjusting regulator parameters such as output voltage, current limits, switching frequencies, and ramp rates to name a few. Furthermore, PMBus offers a rich set of fault detection and response controls as well as numerous status and telemetry features.

Communicating over an I²C physical layer – which is already a common physical layer within SpaceVPX by virtue of the intelligent platform management bus (IPMB) used on the utility plane – PMBus affords the power-supply designer to add a small, low power, host controller to configure, control, and gather housekeeping information from PMBus-enabled converters while reporting all relevant information back to the SpaceVPX chassis controller over utility plane. Although host controller solutions are available, no space-qualified DC/DC converter is presently offered with PMBus capability, representing a prime opportunity to innovate.

Disassembling the SpaceVPX SpaceUM

The SpaceUM is perhaps the most challenging module within the SpaceVPX system to design because of its vast responsibilities that must be handled with limited availability of miniaturized, purpose-built, radiation-hardened components. Some of the primary tasks levied upon the SpaceUM include:

- 1. Muxing all primary/redundant power rails to each logic module (max eight modules per SpaceUM)
- 2. Routing IPMB communications between the selected side A/B chassis controller and fanning them out in a “star topology” to each logic module
- 3. Repeating and fanning out system reset, reference, and auxiliary clocks to each logic module

Figure 2, a simplified high-level diagram of the SpaceUM module, depicts the two independent system controllers and a single block representing the redundant power supplies feeding utility plane signals and all six duplicate power rails to the SpaceUM card, respectively. The SpaceUM replicates all of its inputs to each SpaceVPX logic/payload slot – up to eight slots per SpaceUM card. For simplicity, the diagram only shows signals and power going to a single logic/payload slot card. A sideband set of selection signals are used by the SpaceUM card to select which system controller and power supply it will pass through to the backplane.

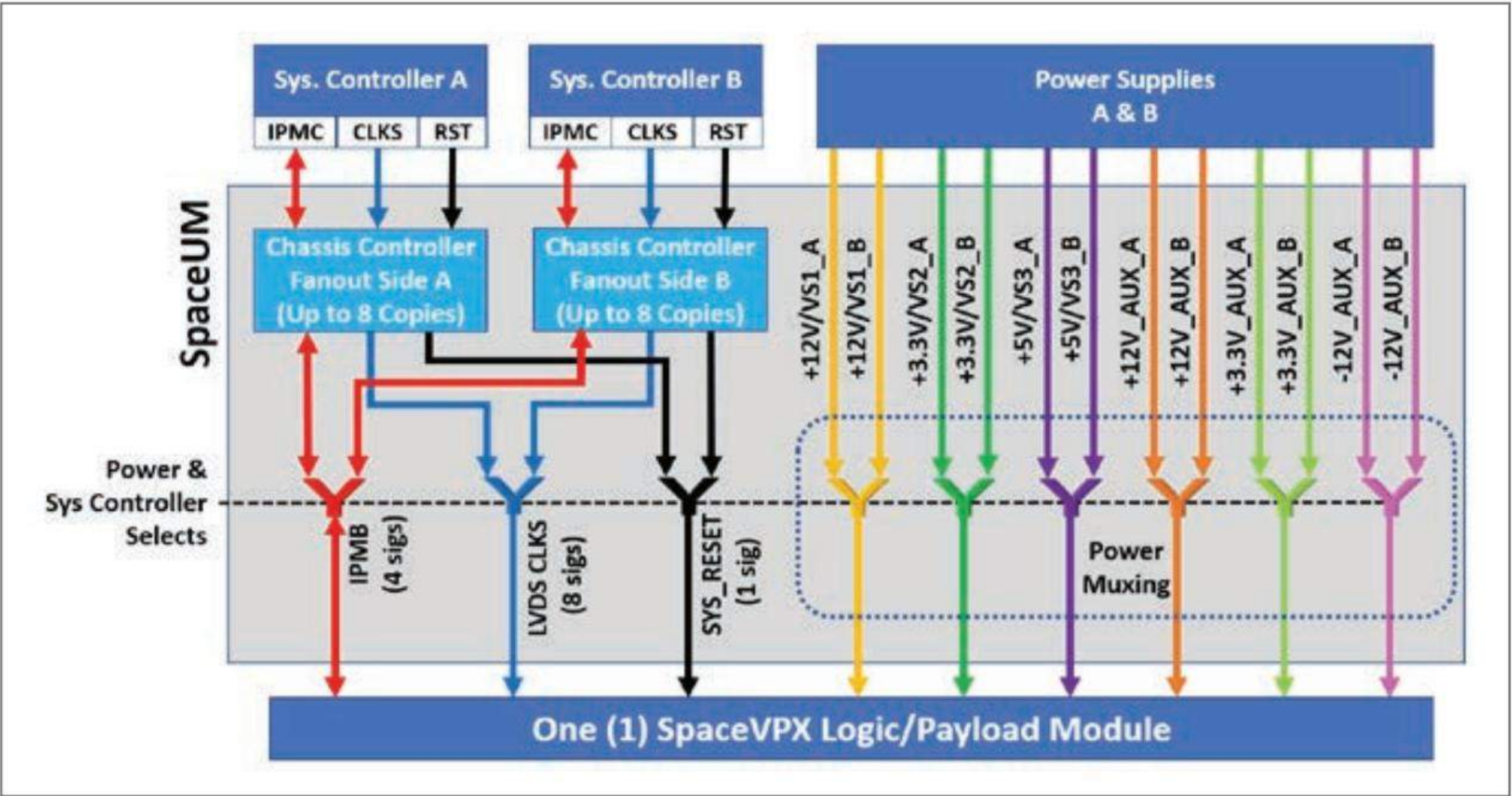


FIGURE 2 | A high-level block diagram shows the layout of the SpaceUM module.

From a component supplier viewpoint, there are a number of interesting functions to serve. Starting with the chassis controller fanout block, the three utility plane signal sets appear fairly simple. At closer inspection, the quantity of signals required for fanout can become I/O-intensive. For example, the IMPB includes four I²C signals per slot. With as many as eight logic/payload slots plus the system controller, the fanout device requires 36 I²C-capable I/O, which quickly outstrips the resources available on all space-qualified microcontrollers. Additionally, the fanout device needs the ability to manage I²C protocol flow control between the system controller and targeted logic/payload slot cards. While the commercial/terrestrial microelectronics solutions include I²C fanout devices, the same cannot be said for rad-hard solutions.

After the utility plane signals have been buffered and fanned out, each side A/B signal grouping must be multiplexed to the plug-in modules through the back-plane interface. The IPMI interface is particularly tricky because the I²C signal characteristics must be retained with bidirectional capability. Unfortunately, the space industry is not presently supported with a true I²C router or multiplexor. Yet, the problem may be solved with transmission gate bus switches. The ideal solution would be transmission gate (T-gate) multiplexors, which don't presently exist in space-qualified formats either, but there are space assured single-pole/single-throw bus switches that can be configured to serve the multiplexing function.

By selecting appropriate channels on the bus switching device, single-pole, single-throw bus switches can be used in a multiplexing configuration. Due to the low series impedance (5 ohms typical) of transmission gates, they offer very fast propagation delay with a high degree of input-to-output signal characteristic matching and natural bidirectional signal transfer.

The next utility plane challenge is routing four differential clock domains to the plug-in modules. The side A and

B system controllers provide a differential system clock, auxiliary clock, and two reference clocks. The SpaceUM modules must receive these clocks and fan them out to each plug-in module using a clock-management device.

The last major responsibility of the SpaceUM modules is switching a plethora of power rails to the plug-in modules, or "power-muxing." Switching a single power rail to a given load is rather simple and straightforward. All that is required is a shunted power MOSFET [metal-oxide-semiconductor field-effect transistor] and gate driver. However, SpaceVPX demands much more.

Power muxing requires reverse current blocking on each redundant power rail, which is generally addressed with a second series shunted ideal diode FET (increasing reliability or power) to block current flowing from the selected supply through the load switch and back into the nonselected power supply. Further, the muxing action requires a selection switch on each rail to connect the commanded supply to the desired payload slot. All combined, a power mux requires up to four power switches and a gate driver/controller for each switch.

Additional considerations affecting the power switching portion of the SpaceUM module include fault detection, isolation and recovery (FDIR); inrush current limiting; current monitoring; and (if desired) housekeeping information on each switched power rail.

Depending upon the current class allocated to each plug-in module, the conductive voltage drops through the switching action can create very difficult design constraints toward meeting the regulated voltage tolerance on each load as well. This is particularly challenging on the 3.3 V and 5 V domains where voltage tolerance is more stringent and current demands are generally higher than what is allocated on the 12 V supply rails.

The space industry offers a fairly broad spectrum of 3.3 V and 5 V power-switch solutions and a slightly narrower range



FIGURE 3 | Smart power-switch controllers enable an agnostic stance on current class, extensive FDIR capability, and integrated telemetry for integrated voltage and current monitoring.

of 12 V switching components. There are no -12 V switch solutions available, leaving it to SpaceUM designers to develop their own discrete -12 V power muxing circuitry.

Focusing on the space-assured power-switching solutions, the designer has several differentiating factors to trade. On the 3.3 V and 5 V rails, some solutions integrate the switching FETs within the controller itself, which favors smaller implementation footprints, but is often current-limited to <10 amps. If the plug-in module is specified for higher current, these devices need to be paralleled up. An additional consideration is fault protection and housekeeping (telemetry) requirements, which are somewhat limited or nonexistent on most of the components.

Alternatively, using devices like the UT05PFD103 (5 V rail) and UT36PFD103 (12 V rail) smart power-switch controllers (SPSCs) empowers the designer with current class agnosticism, extensive FDIR capability as well as integrated voltage and current monitoring telemetry (Figure 3). Using the PMBus interface on the SPSC, the SpaceUM chassis controller fanout-management component can leverage a single I²C port to directly configure, command, control, and gather extensive status and telemetry from every power rail controlled by the SPSCs.

Still, the perfect SpaceVPX power-switching solution does not exist today.

Retaining the manifold advanced features of the SPSCs with embedded power switches supporting >20 amps of current delivery would be a great move toward miniaturizing the SpaceUM power-switching functions. Moreover, adding the power MUX function within a single controller could cut the footprint overhead per switched rail in half. For low-voltage, high-current, power rails the conductive voltage drops must be minimized, which begs for n-channel or GaN power switches for these rails. Finally, a -12 V power-switching solution is an imperative to round out the full SpaceVPX power muxing requirements.

Walk a mile in the designer's shoes

SpaceVPX promises a powerfully flexible, scalable, and fault-resilient platform enabling the highest degree of compute and sensor processing in an open, plug-in

module, oriented system. Delivering on the potential benefits offered by SpaceVPX requires an extensive ecosystem of advanced space-assured components. The space-industry supplier base has innovated many purpose-built solutions to enable successful SpaceVPX implementations, yet more technology innovation is needed to see SpaceVPX realize its full potential.

By standing in the SpaceVPX designer's shoes, component suppliers can quickly learn where the limitations lie. The extent to which component suppliers invest in SpaceVPX-enabling technologies will in turn facilitate more SpaceVPX deployments, resulting in a win-win proposition for both the component suppliers and the system integrators, ultimately providing programs with a flexible, reliable, and scalable platform to implement advanced sensor, artificial intelligence (AI), and computationally intensive applications more quickly and cost-effectively. ■



Tim Meade serves as a systems design engineer for the CAES Space Systems Division. During his more than 20 years at CAES, Tim has held space semiconductor marketing and development positions in the areas of applications engineering, application engineering management, product management, and systems architectural design. He played an integral role in growing the company's semiconductor and system solutions footprint beginning with development of CAES' first space-qualified embedded controller circuit cards, which have deployed on FalconSat-1, CNOF/S, and the International Space Station. Tim studied at the University of Colorado at Colorado Springs where he earned a BS in electrical engineering and an MBA in technology management. Readers may email the author at Tim.L.Meade@CAES.com.

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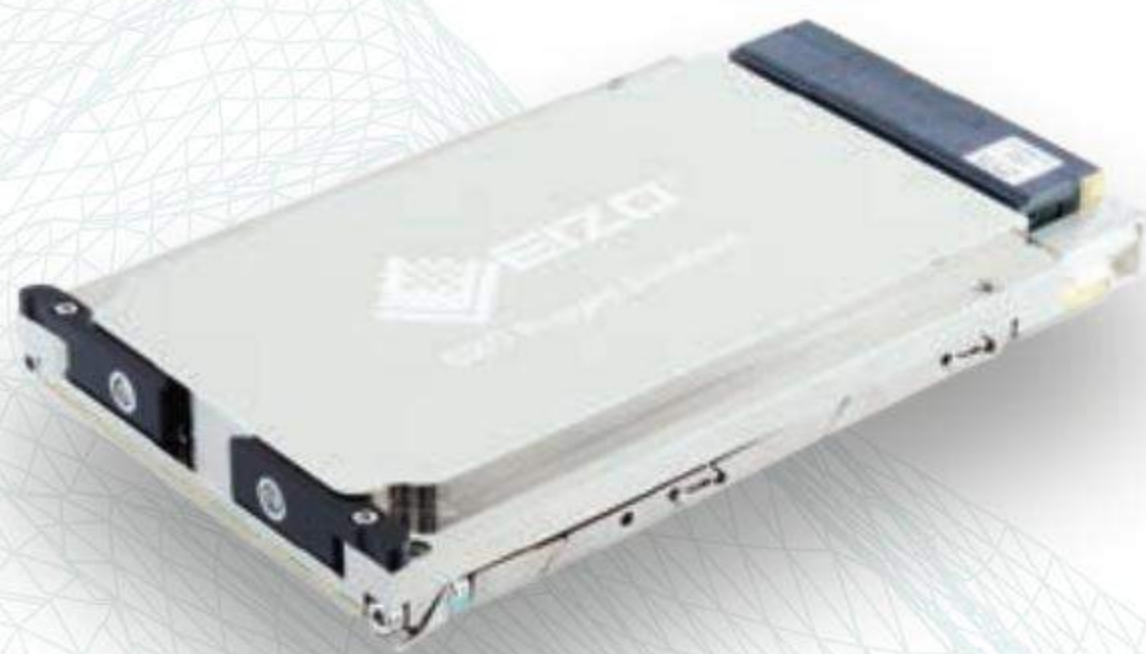
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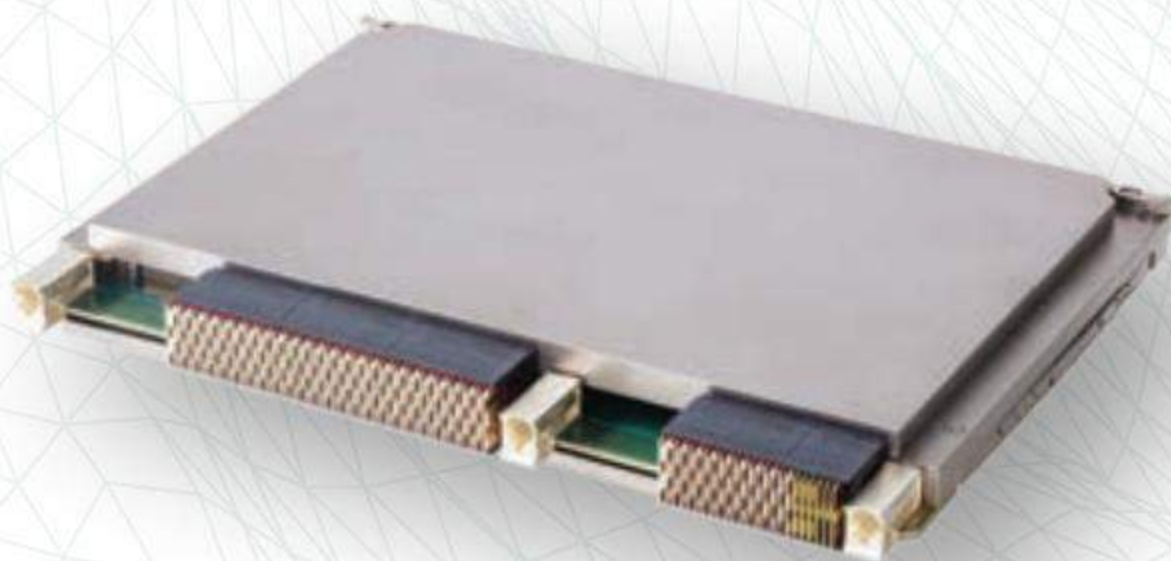
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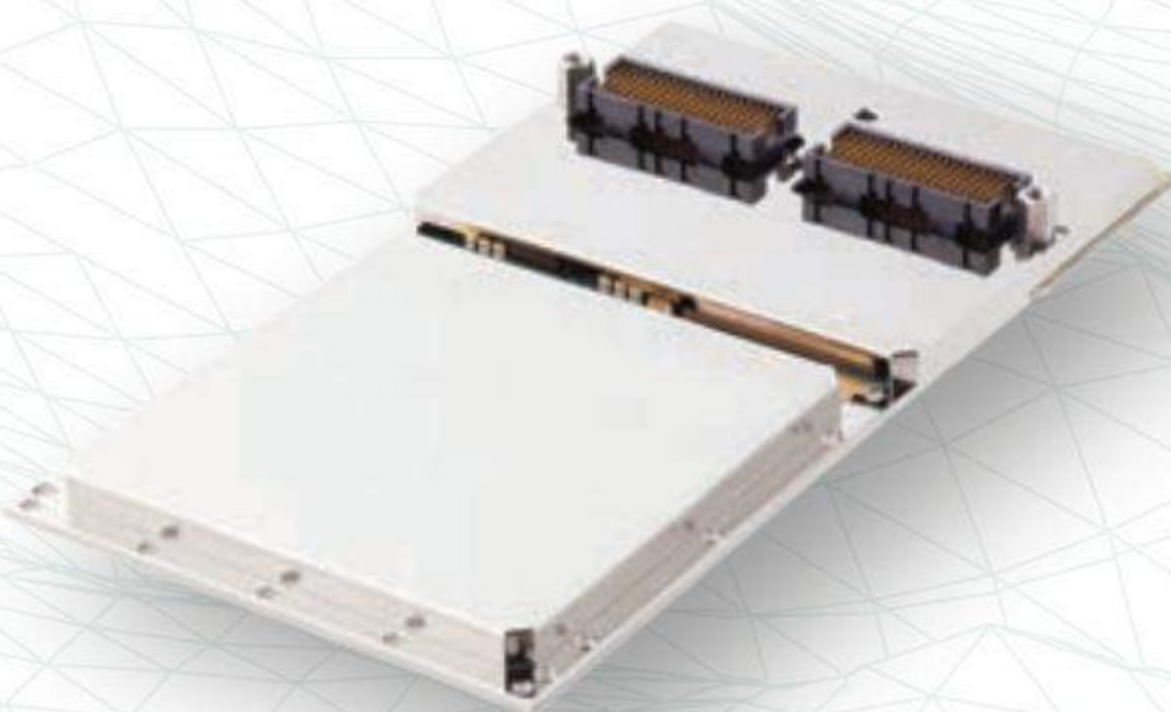
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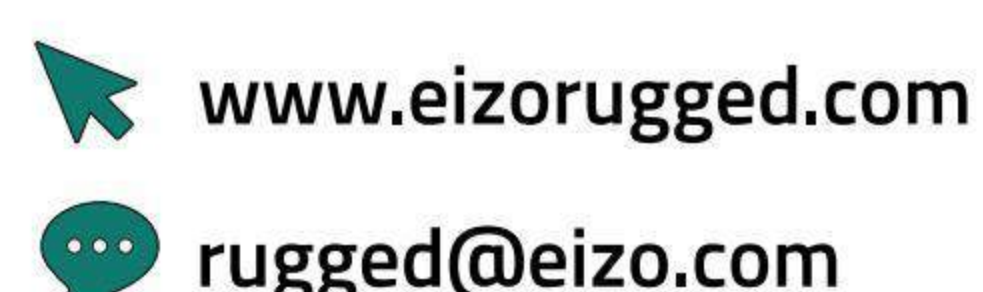
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QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

The SOSA™ Technical Standard Drives Radical Innovation, Including a 64 GSps ADC/DAC Card

By Noah Donaldson, CTO of Annapolis Micro Systems

By narrowing options and better defining specifications that affect interoperability, the SOSA™ Technical Standard encourages innovation and higher performance. Engineering resources that were formerly devoted to myriad design iterations have been redeployed to address radar and electronic warfare system capability.

As an example, VITA 65 OpenVPX allows for dozens of 6U VPX and 3U VPX slot profiles. On the other hand, SOSA™ restricts primary slot profiles to three 6U and six 3U profiles. Restricting the number of profiles significantly reduces the possible backplane configurations, and promotes multi-vendor connectivity.

The SOSA™ Technical Standard also addresses hardware system management, power supplies, maintenance ports, connectors, bandwidth performance, thermal control, and slot pitch.

The SOSA™ Technical Standard doesn't limit, however, performance and capability *within* a module. That's how our focus on being the first to integrate the newest and highest-performing FPGAs and other components has really paid off.

Partnering with Jarjet Technologies, we developed the SOSA™ aligned DME1 Card, the industry's first COTS product to feature 64 GS/s, 10-bit ADC and DAC capability. It is targeted at demanding EW applications requiring direct sampling frequency coverage anywhere from 0.1 to 36 GHz, and/or wide instantaneous bandwidths.

Of course, this huge leap in front-end bandwidth performance requires an upgrade in backplane bandwidth capability. Once again, The SOSA™ Technical Standard comes to the rescue – its working groups are organized to be nimble enough to incorporate this improved backplane connectivity into an upcoming revision.



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EXECUTIVE SPEAKOUT

QUESTION: How does the SOSA™ Technical Standard build on open standards? Pick one and explain: (OpenVPX, HOST, FACE, CMOSS, RedHawk, other.)

The SOSA™ Technical Standard A Subset of OpenVPX

By Jim Tierney, Vice President Aerospace & Defense Systems

At the technical level, the Sensor Open Systems Architecture™ (SOSA™) Technical Standard adopted concepts and definitions from the OpenVPX standard. These concepts and definitions include a taxonomy of planes, pipes, and profiles. Nevertheless, SOSA™ only supports a limited subset of the OpenVPX profile's available options. There are quite a few Plug-In Card Profiles (PICPs) in OpenVPX that are, for the most part, identical. The SOSA™ Technical Standard uses the concept of a pinout "overlay" to define the functionality of previously undefined pins in order to simplify the situation while still allowing for flexibility. This helps to simplify the serviceability.

However, the new standard does maintain flexibility by expanding on the OpenVPX alternate profile module scheme with specific fields for RF pinouts, X memory controller (XMC) overlay, and switch front panel fiber I/O. This is accomplished despite the fact that the number of protocol implementations defined

within OpenVPX is decreased as a result of The SOSA™ Technical Standard.

As an outcome of this, actual SOSA™ systems will have the same appearance as OpenVPX systems, albeit with a significantly reduced amount of adaptability. Cards will be able to communicate with one another regardless of the system they are installed in, and backplanes will be pin-compatible with a wide variety of cards produced by a number of different manufacturers as a result of a much more stringently defined technical specification.



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QUESTION: How does the SOSA™ Technical Standard build on open standards? Pick one and explain: OpenVPX, HOST, FACE, CMOSS, RedHawk, other.

MOSA on the March

By Chris Wiltsey, Senior Vice President and General Manager, Curtiss-Wright Defense Solutions



Last October, we saw the release of SOSA™ Technical Standard 1.0, a real milestone in bringing interoperability to sensor systems. And this year's Tri-Services Open Architecture Interoperability Demonstration (TSOA-ID) saw a significant increase in participants and the number of live demonstrations showing working systems that embrace the key open standards that instantiate MOSA. The MOSA demonstrations that Curtiss-Wright presented showed interoperability with nine different industry partners and featured a wide range of applications, including high-performance processing, tactical battlefield communications, networking, secure data storage, and more. The message is that MOSA is real. MOSA has momentum. Programs of record are demanding MOSA solutions, while MOSA and its related open architectures are now commonly called out in RFPs, which is where the rubber hits the road. For many COTS vendors, the Tri-Services Memo issued by the secretaries of the Army, Navy and Air Force was the highest validation of several decades of our combined efforts. The foundation for MOSA was set in 1994, when Secretary of Defense, William J. Perry launched the COTS Initiative that enabled military

use of commercial electronics. In his memo, "A New Way of Doing Business," Secretary Perry wrote "moving to greater use of performance and commercial specifications and standards is one of the most important actions that DoD must take to ensure we are able to meet our military, economic, and policy objectives in the future." We should all applaud Secretary Perry's prescience and vision. Curtiss-Wright is proud to have helped pioneer the open standards movement. Today, we participate in The Open Group SOSA™ Consortium as a Principal Member, and we are all-in on supporting the SOSA™ Technical Standard and driving a modular approach to sensor system design that lowers the cost of integration and speeds the deployment of new capabilities to address emerging threats.

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EXECUTIVE SPEAKOUT

ADVERTORIAL

QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

The SOSA™ Technical Standard Provides Common Building Blocks for Faster Platform Development and More Rapid Technology Upgrades

By Mark Littlefield, Sr. Manager, Embedded Computing Solutions, Elma Electronic



The SOSA™ Technical Standard is not directly about increasing capability of these sorts of systems. It is about designing systems using a common hardware and software architecture to a) more easily and quickly (and therefore, with less cost) develop complex sensor platforms like radar and electronic warfare, and b) enable rapid upgrades of software or hardware components as technology evolves. By using the common building blocks defined by the SOSA™ Technical Standard, integrators do not have to struggle with custom backplanes and troublesome hardware that was never designed to interoperate, nor be forced to write and validate custom shim software to integrate two incompatible software modules.

From a hardware standpoint, the goal of the SOSA™ Technical Standard is to tame the "wild west" of OpenVPX where, despite the existence of common slot profiles, each supplier has their own set of user-defined pins, essentially ensuring design lock-in. Using The SOSA™ Technical Standard gives the integrator the means to remove a particular plug-in card and replace it with a next-generation plug-in card, not necessarily from the same vendor,

and expect the card to "just work" with the others in the system. Also, since different hardware components advance technically at different rates, this gives the integrator the ability to upgrade those components at the rate appropriate for the hardware in question.

From the software standpoint, the SOSA™ Technical Standard introduces the potential for a modern DevOps-style approach to maintain and upgrade modern defense sensor platforms. Individual SOSA™ modules can be quickly integrated, validated, and fielded using modern DevOps tools. In this way, systems can be almost continuously upgraded, giving the warfighter the latest in tools to draw upon.

Integrators need to approach the SOSA™ Technical Standard for what it provides them with respect to ease of integration, as well as enabling easy future upgrades.

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QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

The SOSA™ Technical Standard – Meeting Today's and Tomorrow's Radar, EW and SIGINT Needs

By Lorin Sandler, Director of Applications Engineering, Epiq Solutions



Anyone reading through the released SOSA™ Technical Standard specification understands the work that has gone into developing the open system architecture which promotes hardware and software compatibility and reuse at many levels. With requirements in place for interfaces, interoperability and control, more effort can now be devoted by developers to expand the feature sets and capabilities for applications. Expanding capability can be achieved in various ways. By relying on common interfaces, connecting several various modules with different capabilities allows construction of sensors capable of executing highly complex signal processing needed for mission critical radar, EW, and SIGINT applications. Alternately, but still relying on common interfaces, developers now have the freedom to drive toward smaller form factors by increasing capability and features on a single card.

SOSA™ based standards are furthering capability expansion with the development of mission model examples. These models allow users to understand typical architectures and they illustrate how a SOSA™ based sensor can fit a specific mission need. As signals

change and countermeasures for those signal types change over time, so too must the functions of an EW system. A SOSA™ module, perhaps a new plug-in-card with increased signal processing features, can provide key processing upgrades in one package as a "technology insertion," which can be easily done in the field with a card swap.

As part of the SOSA™ Hardware Working Group, I can tell you it has been a significant challenge to create a standard that ensures module flexibility yet allows for varying implementation and unique features within the modules while yielding a high-performance sensor meeting the functional requirements of these complex systems. But it is worthwhile work that is changing the future of radar, EW, and SIGINT applications for the better.



EXECUTIVE SPEAKOUT

ADVERTORIAL

QUESTION: How does the SOSA™ Technical Standard impact mission compute applications?

Choices: Interoperability at the Backplane ... or Front Panel

By Chris A. Ciufu, Chief Technology Officer



The root of the SOSA™ Technical Standard is the DoD's Modular Open Standards Approach (MOSA) mandate requiring open standards on most new programs. Open standards benefit the U.S. government (USG) and the DoD by easing the burden on programs by: widening the choices of technologies, vendors and system solutions to C5ISR and mission compute problems, while simultaneously promising a smooth upgrade path over time. As well, open standards have a better chance of minimizing vendor-lock while protecting programs from the inevitable COTS component obsolescence, which is a fundamental part of the integrated circuit (IC) industry and of progressive COTS technology in general. SOSA's™ focus on sensor systems promises vendor interoperability at the slot card level in mission computing systems with a promise of plug-and-play replacement of Vendor C with Vendor M if the ATR or vetronics chassis is cracked open.

While I've never seen this swap successfully accomplished at the demos I've witnessed, the SOSA™ Consortium and we vendors are working diligently to make this dream a reality. The SOSA™

certification process and future interoperability testing will recall the early days of VMEbus "plugfests" which *did* show that swap-outs are possible. Until then, GMS remains a SOSA™ participant with a broad product line of SOSA™ aligned OpenVPX modules and chassis. Alternatively, the GMS X9 small form factor distributed architecture, based on 40Gbps, USB Type-C equipped Thunderbolt 4™ technology, delivers vendor interoperability at the chassis interface with no need to ever crack open the small chassis. Like USB, Thunderbolt 4™ technology is widely used and just works, allowing a GMS X9 Host mission processor to be upgraded or complemented with a completely different X9 or other vendor's module – as long as they all have industry-standard Thunderbolt 4™ interfaces at the front panel.



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QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

How SOSA™ Technical Standard Impacts Mission Compute Applications

By RJ McLaren, Systems Engineering Manager at Kontron

Key Defense initiatives are clearly being achieved based on the work accomplished by everyone involved in the SOSA™ Technical Standard, and the result of this work is being demonstrated in the wide adoption of these SOSA™ aligned products and how they are rapidly being used and adopted in mission compute applications. Kontron is proud of its participation with this group and how it's helping to drive our VPX compute and switch board product offerings and shaping our future roadmaps.

The ability for suppliers to focus on developing core products based on their expertise is providing a rich ecosystem of hardware that Defense Integrators are able to leverage from. Leveraging true standard solutions, instead of modified standard, helps the marketplace achieve better economies of scale and allows vendors to focus more on providing robust solutions instead of trying to modify the products to meet specific mission compute requirements for each program. These stable products are allowing integrators and innovators to rapidly develop and deploy next

generation hardware at a record pace along with providing a growing market for vendors to continue to invest in.

The unique collaboration and results from the SOSA™ Technical Standard provided the necessary guidance in defining the interconnections and requirements between the sensors and the compute hardware which has allowed vendors to develop leading edge hardware to meet these specific needs which in turn has enabled the integrators to develop compact and reliable mission computers for a wide range of applications. Even though it is still relatively early since the release of the SOSA™ standard, the adoption rate and level of interest in these SOSA™ Technical Standard compliant products is making a profound impact in the VPX market.



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EXECUTIVE SPEAKOUT

QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

The SOSA™ Technical Standard – Rapid Deployment of Leading Edge Technology

By Dan Manoukian, President, LCR Embedded Systems

The SOSA™ Technical Standard and the various standards that it incorporates, allows embedded applications to efficiently leverage new off-the-shelf processing, switch, I/O and digitization systems to configure RADAR/electronic warfare systems. This represents a major benefit vs. proprietary system designs that require configuring a new system from the ground up. SOSA™, as a modular open systems approach (MOSA) paves the way for the swift uptake of the latest commercially available technology for use in embedded defense systems. As a result, The SOSA™ Technical Standard has the capability to dramatically reduce the lag time between advances in the commercial electronics and software industry, and their application on the battlefield.

As the RF spectrum becomes increasingly crowded and complex, embedded systems need to stay in step. SOSA™ includes connector and signal speed improvements with the inclusion of VITA 66/67 backplane connectivity for optical and RF I/O and the addition of 100Gb data rates across the backplane. These enhancements enable vast improvements in the signal speed, signal integrity and processing speeds needed to support the changing landscape in electronic warfare and radar applications.

A key benefit of SOSA™ with regard to radar and electronic warfare applications lay in the modularization in software components that increase the capability and flexibility of deployed systems. Software modularization and protocol standardization, enables fast mission re-purposing, system updates and multi-mission functionality as new algorithms are ported to existing platforms intended for re-assignment.

In addition to reducing the time to deployment for new technology, SOSA™ modularity smooths future supply chain issues by ensuring commonality across connectors, chip sets, board sizes and other mechanical/electrical hardware components. This is the SOSA™/VITA promise – extended life of the base hardware while allowing future performance upgrades by utilizing standards based interfaces and certified interoperability supporting commercial technology.



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QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

The SOSA™ Technical Standard Supports Rapid Technology Insertion

By Rodger Hosking, Director of Sales, Mercury

To maintain military superiority over our adversaries, one of the greatest challenges for our defense forces is acquiring new technology in deployable platforms as early as possible. This is especially true for radar and electronic warfare because they both rely primarily on the latest technologies for data conversion, signal processing, and fast interfaces.

Depending on the complexity and performance requirements of these systems, traditional acquisition cycles can span a decade or more, because they often consist of proprietary sub-assemblies designed from scratch. Design reviews, evaluations, and qualification testing consume a major share of such programs. By the time a new system is ready for delivery, its underlying technology is often no longer relevant.

The fundamental objectives of the SOSA™ Technical Standard 1.0, released in September 2021, explicitly address these issues in several ways. The SOSA™ Technical Standard adopts specific sections of existing open standards for embedded systems that can best support the functional and environmental requirements of MIL-AERO systems. For example, only a handful of slot, module and backplane profiles from VITA 65 OpenVPX were selected,

often retaining only certain subsets of each profile. These judicious choices by experts in SOSA™ working groups, consisting of representatives from DoD, the vendor community, and universities, narrowed the number of different 3U and 6U profiles to only a handful. SOSA™ also strongly promotes the use of multi-gigabit Ethernet backplane signal connections and a switch slot to easily reconfigure those connections between plug-in card slots in software.

These initiatives significantly enhance interoperability among plug-in card vendors and reduce the number of different backplanes required across a wide range of applications. Once a SOSA™ aligned plug-in card with critical new technology becomes available, it can quickly replace an older card with the same SOSA™ profile. Because the rest of the SOSA™ system is largely unchanged, the time for qualification, approval and deployment of the upgraded system is dramatically shortened.

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EXECUTIVE SPEAKOUT

QUESTION: How does the SOSA™ Technical Standard enable increased capability for radar and electronic warfare applications?

SOSA™ Technical Standard; The SWaP Advantage

By Brian Paul, General Manager at Milpower Source

Systems integrators are increasingly facing Size, Weight, and Power (SWaP) challenges to achieve new levels of technology insertion for radar and electronic warfare system design. As computing capability improves, the demand for greater performance from radar and EW systems keeps pace in an environment in which the DoD has mandated Modular Open Systems Architecture (MOSA). How does the integrator keep pace?

The SOSA™ Technical Standard is industry's solution to this broad challenge. The SOSA™ Technical Standard improves speed for technology refresh, reduces costs, and increases competition to bring a solution set to this challenge, especially for radar and EW subsystem design. The SOSA™ Technical Standard leverages a network of mechanical, software, and communications standards that mesh this solution space into a tool utilized by integrators. Further, this Standard forces board level manufacturers to think at the system level to ensure interoperability.

One such element adopted by the SOSA™ Technical Standard is VITA 48.8, a standard that defines mechanical parameters for air

flow between VPX boards, an excellent example of how radar and EW system designers can take advantage of open architecture standards while improving SWaP. Utilizing VITA 48.8 compliant 3U and 6U VPX solutions, without the expense and weight of conduction cooled designs, helps achieve weight savings of 30-40%! Ejectors, wedgelocks, and heavy chassis material selections are a few examples where weight savings are achieved. The ability to develop an air cooled chassis within an EW subsystem, for example, provides an opportunity for greater performance in the same volume and equates to increased capabilities for these applications. The Standard has a direct and positive impact on radar and EW design and integration.

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QUESTION: How does the SOSA™ Technical Standard build on open standards? Pick one and explain: OpenVPX, HOST, FACE, CMOSS, RedHawk, other.

The SOSA™ Technical Standard drives next generation sensor solutions and roadmap for future OpenVPX development

By Michael Walmsley, Consultant & Former Global Product Manager, TE Connectivity



The SOSA™ Technical Standard leverages OpenVPX for its hardware element. OpenVPX has been a highly successful architecture for military embedded systems and offers significant capabilities in terms of high speed signaling, power, thermal management with a broad supply base from the chassis to plug-in modules, backplanes, and interconnect.

Specifically, the SOSA™ Technical Standard selected a subset of VITA standard OpenVPX slot profiles and cooling methods to drive volume and interoperability. Each sensor system application – whether a switch, single board computer, RF tuner, etc. – has specific slot profile options within the SOSA™ Standard. These slots are built with interconnect and guide hardware defined by VITA standards, both on the backplane and within the Plug-In Card (PIC).

The interconnect for the OpenVPX plug-in module to backplane interface consists of VITA 46 high speed connectors for power, utility and high speed signaling (currently supporting Baud rates to 32Gb/s). RF and optical connector modules per VITA 67.3 and 66.5 can be integrated into the slot profiles as required. VITA 46

also defines the guide hardware and mechanical structures to assure alignment and intermateability across manufacturers.

The SOSA™ Technical Standard not only adopted OpenVPX as the hardware architecture but drove new developments and standards within VITA to support specific challenges. Examples include new higher density RF and optical connector modules (per VITA 67.3 and 66.5), a higher density optical I/O connector (VITA 87) and new slot profile options (added to VITA 65.1).

There is a continuing evolution of VITA standards for higher speed, higher density, and improved cooling methods which support the OpenVPX ecosystem. With adoption of OpenVPX architecture, SOSA™ can drive next generation sensor solutions by leveraging these new technologies and standards. The SOSA™ Technical Standard can continue to influence the roadmap for future OpenVPX development.



EXECUTIVE SPEAKOUT

QUESTION: How does the SOSA™ Technical Standard build on open standards? Pick one and explain: OpenVPX, HOST, FACE, CMOSS, RedHawk, other.

SOSA™: Building on the success of existing open standards

By David Stone, Executive Vice President, Wakefield Thermal



Adversarial threats in the electronic warfare (EW) and signals intelligence (SIGINT) space continue to evolve and become more complex at a rapid rate. The U.S. response must be just as complex and must ensure that open architectures and commercial solutions can respond quickly to threats as they emerge. This is why the Tri-Service memo mandating a Modular Open Systems Approach (MOSA) for new program designs and refreshes is so critical. MOSA initiatives like the Sensor Open Systems Architecture (SOSA™) Technical Standard enable system designers to adapt open standards like OpenVPX, which leverage state-of-the-art processing and RF technology more quickly and with reduced life cycle costs.

The ways in which SOSA™ builds on existing open standards like OpenVPX are the key to why it stands apart from other similar endeavors. SOSA™ from the beginning strove to adopt existing standards first in order to benefit from years of prior design and development experience. One such standard is OpenVPX, which was developed in the early 2010s by the VITA Standards Organization, also a member of SOSA™. By building on the work of VITA – which has been around for 40 years – developing standards

such as VMEbus as well as ruggedization and thermal management standards and methods that are critical to systems deployed to extreme military environments, SOSA™ leverages all that engineering experience and research.

Another critical component to the success of SOSA™ is the makeup of the consortium, which counts among its members not only the end users – the U.S. military – but also includes the standards organizations like VITA, the prime contractors, system integrators, COTS suppliers, and even chip makers like Intel and Nvidia. In short, SOSA™ represents the whole design cycle from the commercial integrated circuit through systems deployed to the battlefield. That conscious blend will enable open architecture systems to bring the best of the commercial world more quickly and efficiently to the warfighter at the edge of the battlespace.



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CONCURRENT TECHNOLOGIES

TR L9x/6sd-RCx

TR L9x/6sd-RCx has been designed in alignment with the SOSA™ Technical Standard for I/O intensive processor boards.

There are two processor options: an 8-core solution fitted with the Intel® Xeon® W-11865MRE processor; a 4-core solution fitted with an Intel® Xeon® W-11155MRE processor.

Both of these processors come with an integral GPGPU engine with 32 Execution Units which can be used for display or acceleration purposes using OpenCL™, OneAPI or OpenVINO™ for image processing or Artificial Intelligence.



FEATURES

- > Up to 8-core processor for high performance
- > Up to 100G Ethernet Data plane
- > PCI Express Expansion plane for high-speed communication with adjacent board(s)
- > XMC site for additional I/O resources
- > Optional M.2 module for storage with Write/Protect and Opal 2.0 compliance

<https://www.gocct.com/product/tr-l9x-6sd-rcx-rugged-3u-vpx-plug-in-card/>

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A DELTA INFORMATION SYSTEMS COMPANY

Model VPX720 2-CH H.265 Video Encoder

Delta's VPX720 Video Encoder module provides high-quality, low latency full motion video for any ISR application. Whether it is manned or unmanned, airborne, ground-mobile, or shipboard, this module delivers. Providing state-of-the-art video compression in a low SWaP module, the VPX720 is a plug 'n play solution for any SOSA™ aligned chassis.

Based on an advanced multimedia architecture, the Model VPX720 provides real-time video compression for HD/SD video formats in a standard OpenVPX form factor. The VPX720 is a low power, 3U module supporting SMPTE and composite video, complying with the ANSI/VITA 65 standard. Capable of processing two video channels with resolutions to 1080p, the module utilizes H.265 HEVC algorithm providing high quality video transmission with various video resolutions. The module can be configured for a wide range of bandwidths and is especially effective for constrained datalink transmission. Delta's MISB-compliant transport protocol ensures interoperability with down-stream dissemination and exploitation systems.



FEATURES

- > Real-time video compression of HD/SD video
- > Rugged OpenVPX 3U Module, <20W
- > H.265 HEVC / H.264 AVC
- > 3G/HD/SD-SDI or Composite Video Input Interface
- > Aligned with SOSA™, HOST, CMOSS, MIL-STD-810 standards
- > MISB-compliant video, KLV metadata, transport
- > Data Rates from 128Kbps to 25Mbps; <50ms Encode Latency

<https://www.deltadigitalvideo.com/products/rugged-video-encoders/model-vpx720/>

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CURTISS - WRIGHT

3U Plug In Cards (PICs): Payload Profiles –
Compute-Intensive (SBC, FPGA, etc.)

CHAMP-XD3 Intel Xeon D-1700 Secure DSP Engine

The CHAMP-XD3 is a security-enhanced digital signal processing (DSP) engine developed to meet and exceed the needs of modern multi-mode and synthetic aperture radars (SAR), signal intelligence (SIGINT), electro-optical/Infrared (EO/IR), and electronic warfare (EW) applications. Leveraging Intel's latest Ice Lake Xeon® D-1700 architecture, the CHAMP-XD3 maximizes embedded DSP capability by balancing processor performance with memory and I/O bandwidth and having the right features for secure, reliable defense processing applications.

The CHAMP-XD3 couples Intel's AVX512 floating-point capability with 48 GB of high-capacity DDR4-2400 memory via three >19 GBps memory channels for unrestricted, balanced processing power. The third memory bank and wide pipes deliver 50% more memory bandwidth than prior generation modules removing bottlenecks and enabling the Xeon processor to run unrestricted. AI applications critical to cognitive EW and other intelligent sensor processing applications are accelerated using the Xeon processor's built-in Intel Deep Learning Boost capability.

Complementing the main Xeon processor is a Xilinx Zynq® UltraScale+™ MPSoC field-programmable gate array (FPGA), which adds additional security features to Curtiss-Wright's built-in enhanced trusted COTS (eTCOTS) security IP. This sophisticated FPGA also features an embedded quad-core Arm® A53 and dual-core R5 processors for coprocessing and general-purpose I/O processing.

A separate Microsemi SmartFusion FPGA provides an intelligent platform management controller (IPMC) with HOST 3.0 extensions compatibility for system and health monitoring. The CHAMP-XD3

is supported by firmware, operating systems (OS), communication application programming interfaces (APIs), and signal processing libraries.

Aligned to the SOSA™ Technical Standard's compute intense payload profile, the CHAMP-XD3 has a 40GbE data plane, dual 10 GbE, and 16 lanes of Gen3 PCIe expansion plane interfaces for wide-band connectivity with other system processing nodes.

FEATURES

- > Intel Ice Lake Xeon D-1746TER 10-core processor with AI acceleration
- > Three independent memory banks with 48 GB DDR4 SDRAM
- > Two channels of NVMe SSD supporting up to 160 GB SLC/480 GB TLC of secure storage
- > 40 GbE data plane, dual 10 GbE-KR ports, and 16 Gen 3 PCIe expansion plane
- > Base Xilinx MPSoC FPGA Toolkit - RHEL and Alma Linux board support package and driver suite
- > Feature/component/connectivity/memory harmonized for unrestricted, predictable processing power
- > Rugged conduction-cooled packaging and low power for reliable processing in the harshest environment
- > ANSI/VITA and SOSA™ aligned for interoperability
- > eTCOTS and security-enhanced Xilinx Zynq® UltraScale+™ FPGA for mission assurance
- > SmartFusion2 FPGA for next-gen tier 2/3 system management



<https://www.curtisswrightds.com/products/computing/processors/3u-vpx/champ-xd3.html>

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3U Plug In Cards (PICs): Payload Profiles –
Compute-Intensive (SBC, FPGA, etc.)

Sidekiq VPX400

At Epiq Solutions, we push the boundaries of low SWaP software-defined radios (SDRs) based on open architecture and standard form-factors. In using the SOSA™ Technical Standard with our SDRs, we strive to simplify development of mission-critical RF systems like electronic warfare (EW) and signal intelligence (SIGINT) in order to get them into the field as quickly as possible.

Our Sidekiq VPX400 is a great example of SOSA™ standards in action. It is a CMOSS/SOSA™ aligned, modular, multi-channel RF transceiver solution that enables rapid development of converged SIGINT/EW platforms while reducing slot count requirements, power consumption, and engineering-related cost. Its modularity provides rapid adaptability and its core SDR technology future-proofs applications by allowing quick adoption of emerging capabilities.

Sidekiq VPX400 provides a complete antenna-to-bits, phase coherent RF transceiver solution with multi-receive and multi-transmit capabilities in a 3U VPX form factor. Built on Epiq Solutions' proven Sidekiq X4 RF transceiver, the RF front end integrates two Analog Devices ADRV9009 RFICs along with amplifiers and Rx pre-select filters. Sidekiq VPX400 has a wide RF tuning range up to 6 GHz, and can be configured for either 4-channel phase coherent operation at 200 MHz instantaneous bandwidth (IBW) or two independently tunable channels at 400 MHz IBW for a total of 800 MHz IBW. To extend RF frequency access range to 18 GHz, our upcoming Sidekiq VPX410 (July 2022 release) provides an extension solution covering 6-18 GHz. CMOSS/SOSA™ aligned, the Sidekiq VPX410 card is an ideal mate for Sidekiq VPX400.

The high performance Sidekiq VPX400 includes both software and FPGA reference designs that support the Modular Open RF Architecture (MORA) specification, simplifying system integration into any MORA-compliant system supporting for command, control, and streaming digitized I/Q over 10/40 gigabit ethernet to the VPX backplane. With a foundation

in modular open system architecture and flexibility, Sidekiq VPX400 is ideal for expanding system capabilities and functional agility in C5ISR, SIGINT and EW systems platforms while streamlining system engineering efforts and related costs.

FEATURES

- > Complete antennae-to-bits, multi-channel, phase coherent solution in a single 3U VPX card
- > RF tuning range from 1 MHz to 6 GHz
- > 4-channel phase coherent operation at 200 MHz IBW or 2-channel, independently tunable at 400 MHz
- > Unified open API for use across all Sidekiq products
- > Typical power consumption under 30 W
- > Support for both PCIe and 10/40 GbE
- > MORA device layer to allow any SOSA™ aligned host platform to configure and control the card
- > Supports VITA 67.3 for RF I/O through the backplane
- > Air-cooled solution for prototyping, conduction-cooled solution for production
- > Integration with GNU Radio, Photon, MORA, REDHAWK, and other frameworks
- > Conforms to OpenVPX slot profile SLT3-PAY1F1U1S1S1U1U2F1H-14.6.11-4



<https://epiqsolutions.com/rf-transceiver/sidekiq-vpx400/>

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GMS

COMPUTING ENGINES

3U Plug In Cards (PICs): Payload Profiles –
Compute-Intensive (SBC, FPGA, etc.)

X9 Spider VPX

The X9 SPIDER 3U OpenVPX family starts with Intel's latest generation Core i7 CPU Tiger Lake-H processor mounted on a GMS "engine" module. GMS OpenVPX boards using this engine are available in 3U 1-in pitch size featuring IEEE 1101.2 conduction cooling and all offer a massive amount of super-speed I/O never before seen on 3U OpenVPX.

The X9 SPIDER VPX is available in two versions, each of which offers more I/O, processing, and add-on co-processing than is found on two 6U-sized boards (VME or OpenVPX). The 2-slot X9 SPIDER VPX-HS version uses dual 1-inch pitch slots for I/O, power and conduction cooling, and has over 455 Gbps of external bandwidth across 13 ports. The 1-slot (1-inch pitch) conduction-cooled X9 SPIDER VPX-S offers 11 ports and 255 Gbps of I/O bandwidth. Each version represents a complete computer system, replacing two or more 6U modules. This is unheard of for 3U OpenVPX, which is complimented for its small size but then criticized for the lack of user I/O to the backplane. GMS has solved this 3U OpenVPX I/O problem, freeing users to take advantage of 3U's size, weight and power (SWaP) advantages without the limitations of P1/P2 I/O.

The X9 SPIDER VPX-HS and X9 SPIDER VPX-S air- and conduction-cooled 3U OpenVPX single board systems are the fastest, most dense, highest performance compute and I/O processors anywhere in the world. They are developed in alignment with the SOSA™ Technical Standard, follow VITA 65 3U OpenVPX and IEEE 1102.2, and scale up performance and I/O bandwidth, or scale out to other modules and chassis via quad 40Gbps Thunderbolt™ 4 ports, dual 100GigE, or PCIe Gen4 (16Gbps).

As a modular stack, each brings upgradeability, backplane profile independence, and each

offers between 255-455Gbps of interconnectivity to the very highest performing systems. Uniquely, the SPIDER architecture frees designers from the limitations of the OpenVPX backplane while maintaining interoperability with DoD MOSA requirements.

FEATURES

- > Intel® Tiger Lake-H up to 8 cores (2.6GHz, 4.6GHz Turbo Boost)
- > 64GB DDR4 ECC DRAM via upgradeable SO DIMMs
- > Up to massive 455 Gbits/s bandwidth to external I/O
- > x16 and x8 PCIe Gen 4 onboard/off-board inter-connect fabric with optional fiber extender
- > Full size MXM for GPGPU, FPGA, or bus extension
- > 4x Thunderbolt™ 4 ports (40Gbps each) USB-C w/ optional fiber (50m) and 100W+ Power Delivery (each)
- > Dual 100GigE Fiber ports and Dual 10GigE Base-KR to VPX (P1)
- > RAID-capable, quad M.2 sites for storage or I/O
- > 2x USB 3.2 Gen 1 (5 Gbps) via USB-C w/power for console and I/O
- > 1x GigE, 8x GPIO, 2x COM, 2x USB, SATA/PCIe to VPX (P2)
- > Dual SAM™ I/O add-in modules for MIL-1553, ARINC-429, NTDS, GPS, or legacy I/O
- > SOSA™ aligned and U.S. Army CMOSS-ready



<https://www.gms4sbc.com/x9spider>

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mercury

3U Plug In Cards (PICs): Payload Profiles –
Compute-Intensive (SBC, FPGA, etc.)

Model 5553 8-Channel A/D & D/A Zynq UltraScale+ RFSoc Gen 3

The **Quartz® Model 5553** is a high-performance, SOSA™ Technical Standard aligned 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoc. The RFSoc integrates eight RF class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip.

The Model 5553 brings RFSoc performance to 3U VPX with a complete system on a board. Complementing the RFSoc's on-chip resources are the 5553's sophisticated clocking section for single and multiboard synchronization, a low-noise front end for RF input and output, 16 GBytes of DDR4, 10GigE, 40GigE and gigabit serial optical interfaces capable of supporting dual 100GigE

connections and general-purpose serial and parallel signal paths to the FPGA.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The **Navigator FPGA Design Kit (FDK)** includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the installed functions or use the Navigator kit to completely replace the IP with their own.

The **Navigator Board Support Package (BSP)**, the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5553's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 5553 either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

FEATURES

- > Supports Xilinx® Zynq® UltraScale+ RFSoc FPGAs
- > 16 GB of DDR4 SDRAM
- > On-board GPS receiver
- > 10 GigE Interface
- > 40 GigE Interface
- > Dual 100 GigE UDP interface
- > Optional VITA 67.3D optical interface for backplane gigabit serial communication
- > Compatible with several VITA standards including: VITA 46, VITA 48, VITA 67.3D and VITA 65 (OpenVPX™ System Specification)
- > Ruggedized and conduction-cooled versions available



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3U VPX SOSA™ Aligned Software Defined Radio

HTL provides multiple implementations of Software Defined Radio (SDR) in the SOSA™ Technical Standard 3U VPX 3U VPX Payload profile. The SDR provide frequency coverage from 2 MHz to 20 GHz and can be frequency extended to 44 GHz with the external HTL44E. The 80 MHz IBW/channel SDR comes as a 4 channel transceiver covering 2 MHz to 6 GHz (HTLv-13), or as a 2 channel 2 MHz to 20 GHz (HTLv-23). Each channel can be dynamically switched between transmit and receive. Each channel can also be tuned either independently or phase coherently within a module or across multiple modules. The HTLv-63 version is a dual Tx + dual Rx 2000 MHz IBW/channel SDR covering 2 MHz to 20 GHz. Each channel is fixed as Tx or Rx, providing a total of 4 GHz IBW receive and 4 GHz IBW transmit capability. The 6 GSPS ADC/DAC, 1.4 million logic elements, 6.8 TFLOP processing and 4 gigabytes of memory make this product ideal for dual channel DRFM applications or 4 GHz IBW search with 4 GHz IBW EA. To provide more configuration options, the HTLv-63 RF up/down con-



verter and the converter/FPGA modules are available separately. Four of the HTLv-63 in HTL's chassis provides 16 GHz of IBW coverage. All HTL SDR modules support MORA/VICTORY protocol interfaces.

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3U VPX SOSA™ Aligned Graphics Processing Unit

HTL provides two implementations of the NVIDIA 5000 GPGPU on SOSA™ Technical Standard profiles. The first is the HTLv-GPGPU which is a SOSA™ Payload slot aligned GPU providing over 10 TFLOP processing, 3072 CUDA cores, 384 Tensor Cores and 48 RT Cores. The module provides 4 video outputs, 2x as 3G-SDI and 2X as CVBX. The PCIe interface supports over 128 Gbps of IO, sufficient to support over 2 GHz IBW of 16 bit IQ data.

The HTLv-PCIe-GPGPU provides the same 10 TFLOP, CUDA, Tensor and RT processing capability as the HTLv-GPGPU, though it is designed for a switch slot module profile. This profile provides 6 sets of PCIe Gen4 fat pipes (4 lanes) to the module and 8 lanes of 10 Gigabit ethernet. The



3U Plug In Cards (PICs): Payload Profiles – I/O-Intensive (SBC, GPGPU, etc.)

PCIe switch enables a variety of combinations of the PCIe lanes to be interfaced to the NVIDIA 5000 GPGPU. The switch is also interfaced to an optional fiber optic interface to provide routing of signals outside of the chassis.

Multiple modules can be utilized in HTL high performance chassis mixed with RF SDR to create an RF Artificial Intelligence system. Our 19 slot SOSA™ aligned chassis fully populated with these modules can provide over 100 TFLOP of processing capability.

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VX3060-S2/S4

Kontron's VX3060-S2, aligned with the SOSA™ Technical Standard, takes 3U OpenVPX™ to the next level

Featuring 11th Gen Intel® SoC technology, developers can now integrate Kontron's latest 3U VPX blade into their next generation systems

Overview:

Kontron's SOSA™ Technical Standard aligned VX3060-S2 combines robustness, reliability and 15-year-availability with high performance processing, neural network acceleration and powerful graphics capabilities.

CPU SKUs included with the Kontron VX3060-S2 are quad core units supporting specialized Vector Neural Network Instructions (VNNI) and Doubled Signal Processing performance (AVX512). The Gen12 Gfx graphics engine ensures maximum performance for computer vision and media processing – twice that of the previous generation.

Multiple extensions allow developers to more easily address a wide range of demanding mission critical applications. Specific power and temperature monitoring sensors make the VX3060-S2 qualified for safety critical applications. VX3060-S2 can provide Hardware Root of Trust thanks to its TPM module and Kontron SEC-Line elements. The VX3060-S2 pin assignment is compatible with VITA65 OpenVPX Profiles, and the SOSA™ Technical Standard which brings critical new features to existing systems developed in accordance with these standards. A rich Linux™ BSP allows instant evaluation and benchmarking.

Typical Programs:

- Situational Awareness & Imaging Systems
- Vision, Radar, Sonar, or Signal Acquisition & Processing Systems
- Autonomous or Semi-Autonomous Systems
- Supporting Long Term Lifecycle & reliability in harsh environments

Additional Features and Advantages:

CYBER SECURITY, SECURE DEPLOYMENTS

VX3060-S2 design is compatible with the Kontron SEC-Line offering and featuring two secure elements, TPM and AppProtect. TPM supports, measured boot and hardware protection of crypto keys.

System Management with an integrated CPLD and support for VITA 46.11 included. PBIT and CBIT provide power-on-built-in-test features with "basic" and "expert" mode to allow developers flexibility in what features to measure before the OS boot sequence.

FEATURES

- > 11th Gen Intel® Core™ processor for AI, CVGIP, and DSP
- > 12-28 W Quad Core™ processor, Enhanced AI, AVX-512, 32 GByte ECC memory
- > 8k Multi-Head display from Gen12 / 96 EUs high End GPU
- > Versatile I/O: USB-C, M.2 sockets, XMC option
- > Quad core units with Artificial Intelligence (VNNI) and Doubled Signal processing performance
- > The VX3060-S2 comes in two variants, rugged air cooled version and rugged conduction cooled version
- > One variant has three rear ETH BaseT, the other features a dual 10GBaseKR



<https://www.kontron.com/en/products/vx3060-s2/p160535>

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M4154

FIRST TO MARKET

Milpower Source, Inc recently announced the launch of the new M4154 series SOSA™ Technical Standard Aligned 3U VPX DC to DC power supply utilizing air flow through (AFT) cooling technology, compatible with the 3U 1.5" form factor defined in the ANSI/VITA 48.8 standard. This is the first and only 3U air-cooled DC-DC power supply available on the market. Compatible to the VITA 62 mechanical standard, the M4154 can achieve an output of up to 800W of DC power, with a wide input range from 18 to 50VDC, compliant to both air and ground standards for power: MIL-STD-704 and MIL-STD-1275.

The innovative mechanical design coupled with Milpower Source's unique electrical layout expertise offers a rugged, tailorable, and reliable power solution for integrators developing air-cooled electronic warfare, mission computing, processing, radar, or other high-performance applications for military and aerospace applications. The VITA 48.8 standard for Air Flow Through cooling offers the industry a standardized open systems architecture solution to improve SWaP in weight and space-constrained applications. Air flow through cooling methodologies allows for improved reliability through thermal management and reduces the complexity and cost of the system design. The M4154 series power supply offers systems architects a reliable, rugged, and efficient solution to optimize the performance of their embedded computing design with the use of AFT technology.

Milpower Source offers the industry's most complete line of 3U and 6U tailorable VPX powersupplies, including DC-DC, AC-DC, and dual input solutions in VITA, SOSA™ Aligned, and customizable configurations.

FEATURES

- > **FIRST TO MARKET:** Compatible to VITA 48.8 AFB for 3U VPX
- > Aligned with the SOSA™ Technical Standard for 3U VPX w/ AFB Cooling
- > Industry Leading Power Density: Up to 800W Output Power
- > Wide input Range: 18 to 50VDC Standard Version Input
- > Operating Temp: -55°C to +85°C (No Derating)
- > Environmental: MIL-STD-810H
- > Integrated EMI Filters: Complies to MIL-STD-461G
- > System Management: Per VITA 46.11 Tier II
- > Fixed Switching Frequency (220 kHz)
- > Reverse Polarity, Overvoltage, & Indefinite Short Circuit Protections
- > Over Temperature Shutdown with Auto-Recovery



<https://milpower.com/products/power-conversion-solutions/dc-dc-power-supplies/m4154>

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☎ 603-267-8865

CONCURRENT TECHNOLOGIES

PR A11/6sd-RCx

Designed in alignment with the SOSA™ Technical Standard, PR A11/61d-RCR provides resilient PNT data for sensor-based solutions that are used in Electronic Warfare and Intelligence, Surveillance and Reconnaissance applications. As a key differentiator, PR A11/61d-RCR is ITAR free and is designed and built in the UK utilizing technology licensed from Racelogic, another UK company specializing in positioning data.

In normal operation, PR A11/61d-RCR sources highly accurate PNT data from a built in GNSS receiver and uses this to discipline a Chip Scale Atomic Clock (CSAC). This, in turn, feeds radial clock signals to the signal processing plug in cards that make up a VPX based sensor subsystem. In periods of GNSS denial or jamming, accurate PNT data continues to be provided by utilizing signals from a built in Inertial Measurement Unit and sophisticated Kalman filtering techniques. The timing slot on most commercially available backplanes supports one or two 10GBASE-KR pipes and PR A11/61d-RCR is controlled using one or other of these pipes. Bussed clock signals are also supported for backwards compatibility with older VPX systems.

<https://www.gocct.com/product/pr-a11-6sd-rcx-rugged-3u-vpx-position-navigation-and-timing-card/>

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in www.linkedin.com/company/concurrent-technologies-plc/



FEATURES

- > 4-core ARM processor for control and management
- > Integrated multi-constellation, multi-frequency GNSS module with interference and jamming mitigation
- > Chip Scale Atomic Clock (CSAC) and Inertial Measurement Unit (IMU) for assured Position Navigation and Timing
- > Differential radial clock distribution
- > Coaxial Antenna and Timing signals in P2 aperture



SOSA™ Aligned Position, Navigation and Timing (PNT) Module

HTL PNT modules include the PNTRv3 and PNTRv23. The PNTRv3 is Snapshot 3 (Release 1) aligned and provides GPS receiver, GPS/CSAC trained 1 PPS & 100 MHz reference which can be sent to each slot in a SOSA™ aligned chassis. Both modules provide VICTORY/MORA interfaces and have robust PNT capabilities. The PNTRv23 provides additional robust PNT capability including AltNav. Contact HTL for further details.

KEY FEATURES AND SPECIFICATIONS

- Provides low noise 100 MHz reference using Low Noise Chip Scale Atomic Clock (LNCSAC)
- Integrated inertial navigation system (INS) with GPS
- 100 MHz outputs
- Output 1 PPS synchronous to 100 MHz
- On board antenna switching to devices
- 1 GbE Control Interface to OpenVPX Backplane

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3U Plug In Cards (PICs): Radial Clocks – Position, Navigation & Time (PNT) and Timing & Synchronization



VPX NVME and SATA SSD Modules

Add 20TB of data storage to your VPX system!

Red Rock Technologies provides a range of 3U VPX SSD products using COTS SATA and NVME SSDs with capacities up to 20TB and transfer rates up to 7877 MB/S. Air and conduction cooled options.

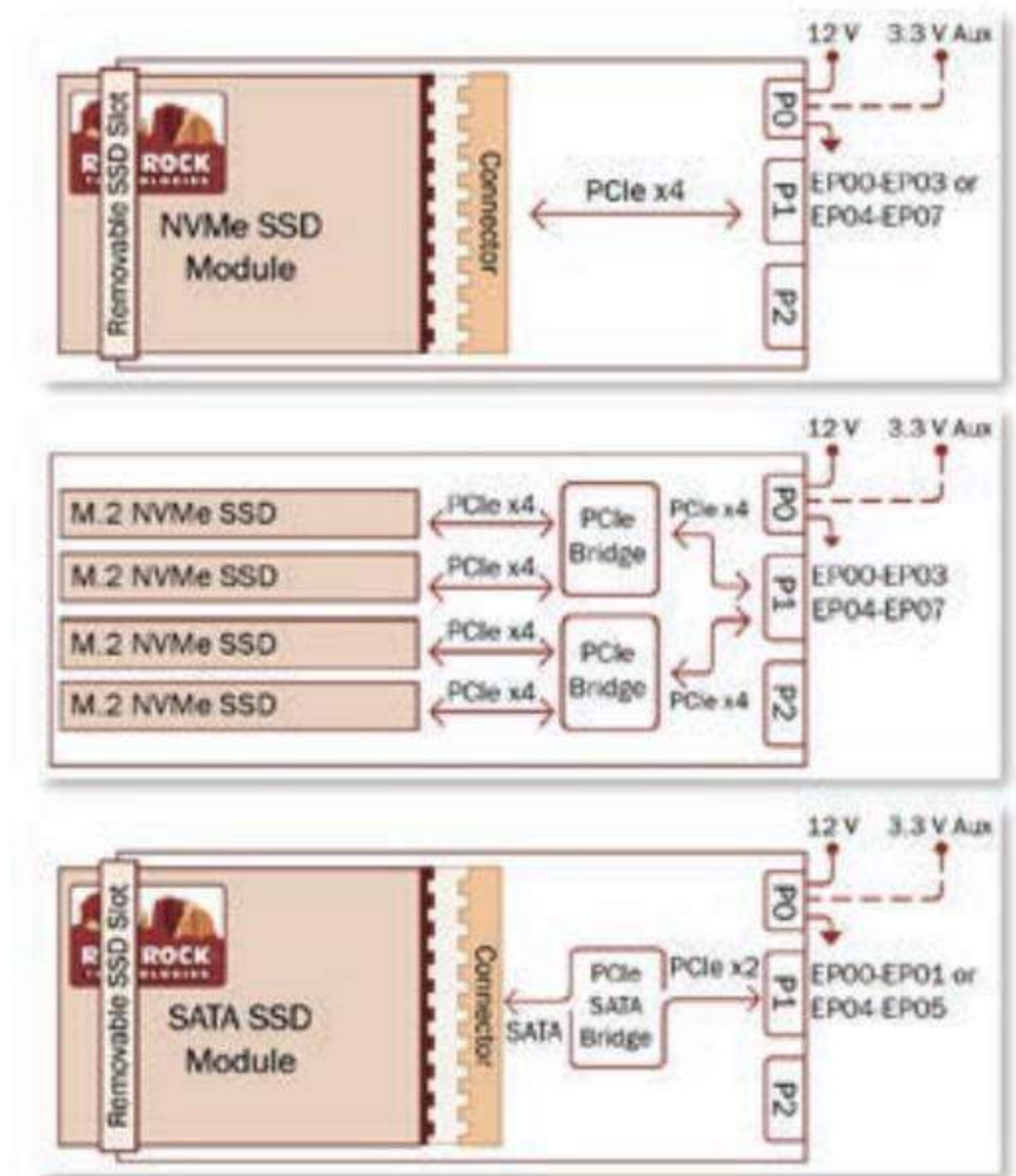
SOSA™ Technical Standard Aligned to use standard VITA 65 3U Payload Slot Profile: SLT3 PAY 1F1U1S1S1U1U2F1H 14.6.11. One or two OpenVPX Fat Pipes (FP) on Expansion plane:

- VPX P1 EP00-EP03 PCIe x4 Interface1
- VPX P1 EP04-EP07 PCIe x4 Interface2

NVME SSDs use PCIe x4 interface on VPX connector and connect directly to NVME SSD. Transfer rates of 7877 MB/S.

SATA SSDs use PCIe x2 interface on VPX connector. The PCIe interface connects to a PCIe SATA controller. Transfer rates of 600 MB/S.

Options with removable SSD modules are rated for 100,000 mating cycles for applications that require frequent removal of SSD. Removable SSD modules can easily be transferred between VPX system and PC.



FEATURES

- › Capacities up to 20TB
- › Removable SSD module rated for 100,000 mating cycles
- › COTS SSDs
- › VxWorks, Linux, and Windows support
- › Requires only +12V and +3.3V Aux power
- › No Tools option with easily removable thumbscrews
- › Military erase, FIPS140-2, FIPS197, TCG Opal options

<https://www.redrocktech.com/products/vpx>

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Dawn SOSA™ Products

Your SOSA™ Partner, Today and Tomorrow.

The acceleration of new technology demands our deployed platforms evolve into adaptable systems.

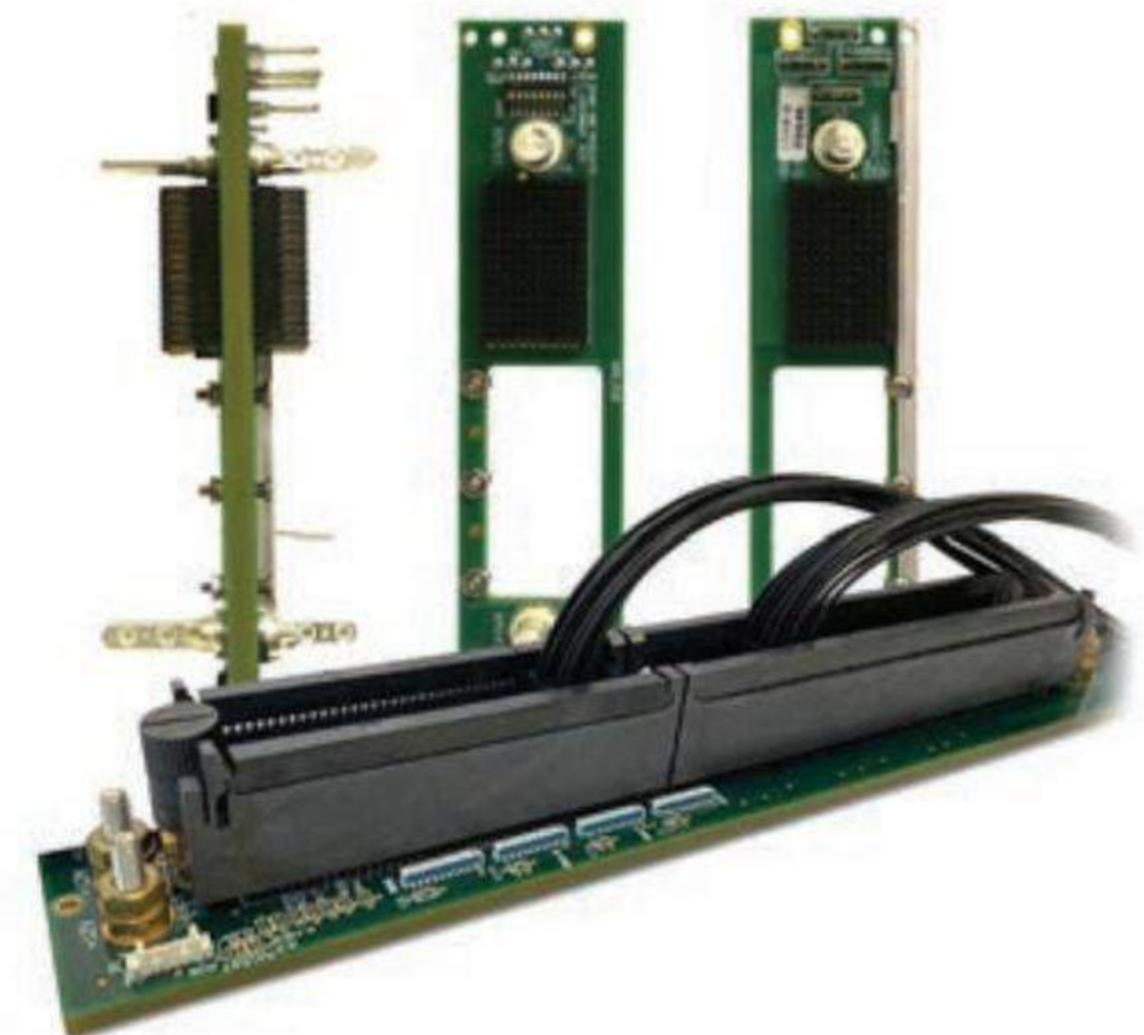
Sensor Open Systems Architecture™ (SOSA) transitions sensor systems to expedite interoperability, reuse and disruptive agility. OpenVPX-based SOSA™ facilitates subsystem SWaP-C improvements and rapid technology upgrades.

To implement new technology faster at reduced cost is a core priority at Dawn. Dawn VME Products is committed to leadership in SOSA™ modules and infrastructure.

We can modify our existing platforms, or incorporate your requirements into a customized solution for prototyping and development. We are dedicated to maximizing customer satisfaction through on-time delivery of zero-defect products.

Rugged, reliable and ready. You need it right. You want Dawn.

Basic specs on some of our available SOSA™ aligned products are shown here.



Backplanes (3U & 6U)

FEATURES

- › VPX-0354 25Gbps SOSA™ 14.2.16 Single Slot Backplane
- › VPX-0557 25Gbps SOSA™ 14.6.11 Single Slot Backplane
- › VPX-0650 25Gbps SOSA™ 14.8.8 Single Slot Backplane
- › VPX-9909 6U VITA 67.3 J3 & J6 Single Slot Backplane
- › MERITEC VPX3 Deployable Backplane
- › Hercules to VPX3 Cabling solution allows speeds of 25 Gb/s+ per line

www.dawnvme.com/sosa-products/

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ELMA

Your Solution Partner

12-Slot 3U Backplane Aligned to the SOSA™ Technical Standard 1.0 and CMOSS

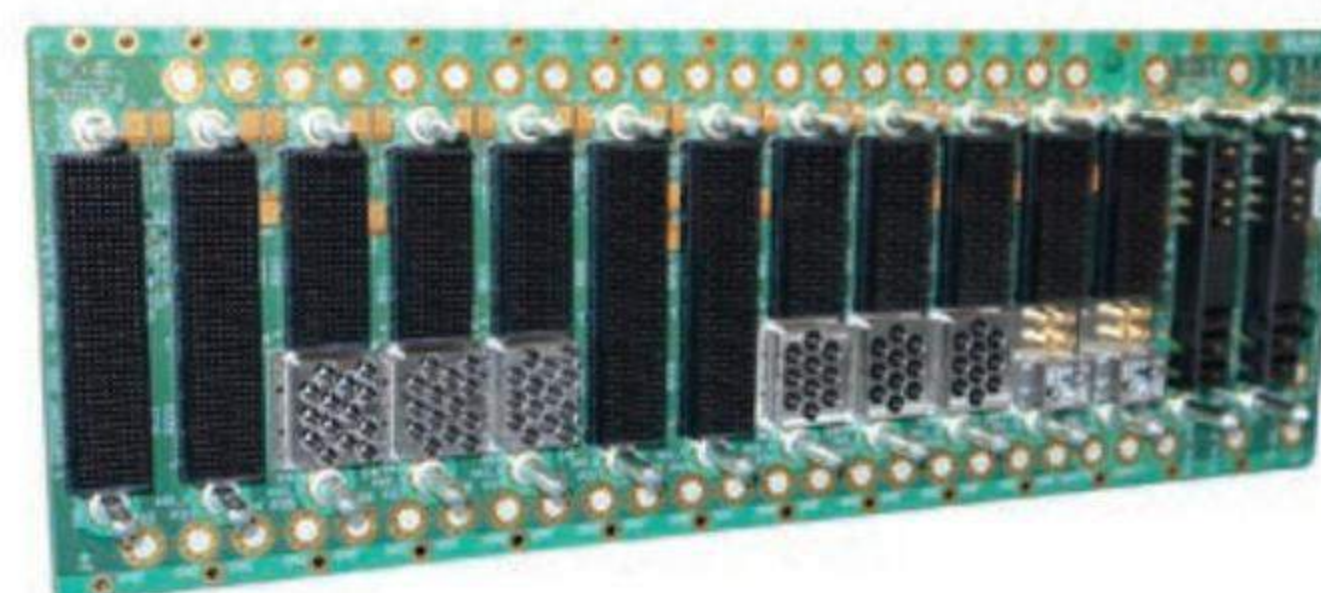
Designed to align with the Sensor Open Systems Architecture™ Technical Standard (SOSA™), this 3U backplane offers 12 plug-in card (PICs) slots to support the defense industry's hardware and software convergence initiatives per the DoD's Modular Opens Systems Approach (MOSA) and meets the U.S. Army's latest CMOSS guidelines. It provides the foundation for high-performance mission-critical systems requiring lower lifecycle costs and rapid technology insertion.

The backplane provides complex, high speed signal processing systems with the latest optical fiber and RF connectivity as well as precision network timing (PNT), plus slot profiles for SBCs, switches, radial clock(s) and expansion.

High-speed signals are supported on all data paths with options for VITA 67.3 connectors and VITA 66.5 optical and hybrid RF/optical connectors.

Developers can use the development backplane as configured or work with Elma to identify specific profile configuration needs.

Backplanes: (3U & 6U)



FEATURES

- > Payload, Switch & PNT slot profiles in alignment with SOSA™ technical standard 1.0
- > Supports 12V-only & +3.3V AUX (SOSA), or full VS rails (legacy)
- > Two VITA 62 Plug-In Power slots
- > Supports dual-domain Ethernet switching 1/10/40 & 25/100
- > PNT slot profile SLT3x-TIM-2S1U22S1U2U1H-14.9.2
- > Maintenance, serial ports, GPIO and CLK1 signals
- > IPMC header for external chassis manager

<https://bit.ly/SOSA12bkp>

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SOSA™ Aligned 3U VPX Chassis

Two SOSA™ aligned 3U VPX chassis are provided by HTL.

The HTLv-C3-11 is an 11-slot chassis with:

- Four Payload slots
- Two PCIe Gen4 switch slots
- 100 Gbps switch slot
- IOSBC slot
- Radial clock slot
- Two power supply slots.

The HTLv-C-19 is a 19-slot chassis with:

- Eight Payload slots
- Two PCIe Gen4 switch slots
- Two 100 Gbps switch slots
- IOSBC slot
- Radial clock slot
- Three power supply slots



Backplanes (3U & 6U)

The VPX conduction cooled modules are in an environmentally sealed enclosure which is cooled via forced air flowing over external fins providing the capability to cool up to 125 Watts per slot at 60 °C ambient temperature. The chassis are designed for rugged environments per MIL-STD-810 and RTCA DO-160 profiles. The operating temperature range is -40 °C to 60 °C.

Using available SOSA™ aligned modules, hundreds of configurations are available, including 16 GHz IBW spectral search engine, 8 GHz spectral search with 8 channel precision DF and 100 TFLOP edge computing. Additional details can be provided upon request.

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VPX stacking compliant pin connector

TE Connectivity's (TE) VPX stacking compliant pin connector matches the footprint of the MULTIGIG RT 2 and MULTIGIG RT 2-R connector and boasts a 4 mm and 4.4 mm stack height, which fits VITA 46 half modules. The connector system allows customers to cable off of the backplane or plug-in card for rugged embedded computing applications. The VPX stacking connector is versatile enough to be used as a half module or stackable side by side to fill a full connector position. With compliant pin termination on both sides, the connector is well suited for rigid flex or board-to-board stacking where a separable interface is not required. The VPX stacking connector also makes installation simple with its press-fit application. TE's stacking connectors are engineered to perform in environments where small, lightweight and rugged connectors are critical for reliability in harsh and strenuous conditions.

FEATURES

- > VITA 46 plug-in card and backplane footprints
- > 4 mm and 4.4 mm stack height
- > Engineered to fill full and partial slot profiles
- > MULTIGIG RT 2-R press-fit contact system
- > Allows users to cable off the backplane or plug-in card for rugged, embedded computing applications
- > Well suited for rigid flex or board-to-board stacking where a separable interface is not required
- > Simple installation with its press-fit application

<https://www.te.com/vpx-stacker>

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🐦 @TEConnectivity

in www.linkedin.com/company/te-connectivity/



SMPS 19 Port Backplane Module – Aligned with the SOSA™ Technical Standard

SV Microwave's SMPS 19 Port Backplane Module C, Aperture H (part number SF9321-60093) aligns with the VITA 67.3 specification in that the floating contacts have been moved to the Backplane side (versus the Plug-in side in 67.1 and 67.2). In order to support design flexibility, increased data rates and high density requirements of VPX platforms, SV has designed this full-width, 19 Port Backplane Module with its smallest high performance interface – the SMPS series. The SMPS series provides excellent electrical performance from DC to 40 GHz and is used extensively in some of the most demanding MIL-AERO programs. The SMPS interface is currently being adopted as a DLA standard under the name SMP3.

The SMPS 19 Port Backplane Module C, Aperture H is aligned with the SOSA™ Technical Standard and works with the below products:

- Plug-In Module: SMPS VITA 67.3 19 Port Plug-in Module C, SF9311-60171
- Contact: SMPS VITA 67.3 Backplane Contact for Ø.086" and Ø.047" cable, 3821-40024 and 3821-40023

In stock through distribution now!

Connectors & Cabling: Board Level Connectors
("VITA 66, 67, ..." or "Optical, RF")



FEATURES

- > Backplane Model
- > 19-Port Configuration
- > SMPS RF Series
- > Module C - Full Width
- > Compatible with .047" and .086" cable types
- > VITA 67.3
- > Aligned with the SOSA™ Technical Standard

<https://svmicrowave.com/smps-vita-673-19-port-backplane-module-c>

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Deployable CMOSS MOSA System

This HPEC ATR system for 3U SOSA™ Technical Standard aligned payloads is intended for RADAR, SIG-INT, EW and EA applications. The rugged design offers an ample I/O complement including multiple receiver and transmitter channels plus 1PPS and 10MHz Ref with a 10Gigabit Ethernet Fiber data interconnect making it an ideal C4ISR Modular Open Sensor Systems (CMOSS) for harsh environments. The system leverages LCR's 800 Series chassis for VITA 48.2 conduction cooled modules with 8 payload and 2 VITA 62 PSU's and removable drive.

LCR integrates a high performance Intel Xeon processor and Nvidia GPGPU providing nearly 10TFLOPs of computational power for high bandwidth I/O requirements in mission critical deployments. Each FPGA sub-system has backplane Ethernet connections to a 40 GigE switch providing copper or optical I/O through 38999 connectors to the front panel. The FPGA sub-system has a full meshed 40Gigabit network between each module. It is designed to accommodate best-in-class 3U CMOSS and SOSA™ aligned payloads to meet mission needs with minimal time to theater.

LCR Embedded Systems
www.lcrembeddedsystems.com

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in www.linkedin.com/company/lcr-embedded-systems-inc-/

☎ 215-760-9909

🐦 @LCREmbedded

Enclosures: Deployable



FEATURES

- > Rugged ATR chassis accommodate best-in-class 3U CMOSS and SOSA™ aligned payloads
- > Integrated systems with SOSA™ alignment to the connector level
- > Intel Xeon D processor with 576GFLOPs performance
- > NVIDIA Pascal GP104 with 2560 CUDA cores and 8.7TFLOPs performance
- > Scalable Xilinx FPGA and tuner subsystem with VITA 49 IF packet compliance
- > 40Gigabit layer 2/3 Ethernet Switch for fiber or copper I/O and removable drive bay
- > Cooling for up to 575W of total power

<https://www.lcrembeddedsystems.com/>

ELMA

Your Solution Partner

3U 12-Slot Development Platform for SOSA™ Technical Standard 1.0 & CMOSS PICs

This 3U OpenVPX development platform provides slot profiles aligned with the Sensor Open Systems Architecture™ (SOSA) Technical Standard 1.0. It supports the latest profiles used to develop systems that follow the hardware requirements of both SOSA™ and CMOSS (C5ISR/EW Modular Open Suite of Standards).

At the heart of the system is Elma's 3U 12-slot OpenVPX backplane (2 I/O intensive SBC slots, 7 primary payload slots, 1 radial clock, 2 switch and 2 power slots) aligned to the the SOSA™ Technical Standard 1.0 and CMOSS. The backplane features VITA 67.3 RF and optical I/O modules for high speed connectivity.

Streamline your development efforts and shorten your time to deployment. Payload boards are available as part of the platform. Choose from a growing ecosystem of processor, network, network timing and power supply modules designed to align with the SOSA™ Technical Standard 1.0 and CMOSS.

<https://bit.ly/12-SOSACMS-DP>

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Enclosures: Development/Test



FEATURES

- > 12-slot 3U backplane aligned to SOSA™ and CMOSS
- > Elma's built-in VITA 46.11 Chassis Manager for intelligent system health monitoring
- > Mix & match slot guides for conduction- and/or air-cooled boards
- > Front panel on/off & reset switches, voltage LEDs; test points; NVMRO & Zeroize switches
- > Maintenance ports routed to connector on rear of backplane, brought out via breakout cable for board
- > Option for SOSA™ 12V power rails or legacy VS rails
- > Choose from a range of partner-tested Plug-In Cards (PICs) aligned with SOSA™ profiles



Enclosures: Development/Test

524 Open Series Development System

3U 11 Slot Open Series Development System, with Slot Profile Aligned to the SOSA™ Technical Standard

The 524 Open Series development system from Atrenne offers a feature-rich design that combines functionality and flexibility with aesthetic detail.

Designed with the engineering developer in mind, the 524 Open Series development system incorporates a 9 slot OpenVPX Backplane (9 payloads + 2 power slots) with profiles aligned to Sensor Open Systems Architecture™ (SOSA) and CMOSS (C4ISR/EW Modular Open Suite of Standards) initiatives.

Unobstructed accessibility to cards under test is enabled for probe access with intelligent system monitoring capabilities. The front of the 524 Open Series development system chassis is configured with LEDs for each voltage and a corresponding test jack for ease of monitoring DC voltages and probing. An AC on/off switch and a system reset switch are also accessible via the front panel.

The 524 Open Series development system incorporates innovative thermal capabilities via the high-performance fans which are placed below the card cage to produce maximum unrestricted airflow while using side-entry air plenums. No matter where the test station is placed, the station will provide optimal cooling required for some of the most demanding cards aligned to SOSA™ manufactured today. The 524 Open Series development system can be configured with a system monitoring board (SMB) with an LCD display. The SMB provides system fan speeds, DC voltage outputs, and monitoring for two temperature sensors. External access to the SMB is available through a rear-mounted USB connector or an optional RS-232 port.

FEATURES

- > Open frame for easy card access
- > Maximum unrestricted airflow and cooling for high-powered cards
- > Supports air-cooled modules using IEEE 1101.10 card guides
- > Supports 3U x 160mm Modules
- > Supports air-cooled modules using IEEE 1101.10 card guides
- > Supports conduction-cooled modules using VITA 48.2 aluminum slot guides
- > Front mounted LED Array for DC Voltages
- > DC voltage test jacks
- > Front mounted power switch and system reset switch
- > High volume, speed-controlled cooling fans
- > Fan fail monitored
- > System Monitoring Board with LCD display



https://www.atrenne.com/products/524?utm_source=mes&utm_medium=media&utm_content=wbp&utm_campaign=st_sosa

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 in www.linkedin.com/company/atrenne-integrated-solutions



100GbE SOSA™ Aligned Development Kit – WS3A01-S1

This next-generation 3U OpenVPX Benchtop Development Platform is both SOSA™ aligned and 100Gb Ethernet capable, and is designed from the ground up to economically speed development of 100GbE applications that are aligned with the SOSA™ Technical Standard.

The stock Kit includes a 3U Chassis, Backplane, Chassis Manager, FPGA Board, 100GbE Switch, SBC, VITA blocks, and MIL-DTL-38999 cable.

For a virtual or in-person Demo, contact us.

OVERALL SYSTEM FEATURES

- Front-loading, air-cooled system with conduction-cooled boards
- Seven 3U OpenVPX slots with SOSA™ aligned backplane profiles
 - One 14.6.11 Payload
 - Three 14.6.11 Empty Payload (for expansion)
 - One 14.2.16 I/O-intensive SBC
 - One 14.4.14 100GbE Switch
 - One VITA 62 Power Supply – 12V-Heavy
- 25 Gbps Line Rates on Data and Expansion Planes
 - 25/40/100Gb Ethernet
 - SDR/DDR/QDR/EDR InfiniBand
 - Gen 3/4 PCI Express
 - Custom protocols up to 25Gbps per lane
- VITA 66.5C and VITA 67.3C for payload slots
- Four MIL-DTL-38999 SOSA™ aligned circular connectors with 19 RF connections, and one MIL-DTL-38999 Cable
- Multiple levels of hardware and software security

CHASSIS MANAGER

- SOSA™ aligned and VITA 46.11 compliant
- Enables control, maintenance, and security functions
- One Xilinx® Zynq® UltraScale+™ MPSoC (XCZU5EG)
- Supports MIL-STD-1553

100Gb ETHERNET SWITCH

- 40/100Gb Ethernet Data Plane Switch
 - 6.4Tb/s switching capacity
 - Industry-leading, true cut through latency
- 1/10/25/40/100Gb Ethernet Control Plane Switch
 - Layer-2 Wire-Speed Switching Engine
- Two Xilinx Zynq UltraScale+ MPSoCs (XCZU5EG)

FPGA PROCESSOR + I/O CARD

- One Xilinx Virtex® UltraScale+ FPGA (XC7VU7P)
- One Xilinx Zynq UltraScale+ MPSoC (XCZU7EV)
- **ADC/DAC Option #1:** Xilinx Zynq UltraScale+ Gen3 RFSoc
 - ADC: 4 Channel, 5.0+GSps Sample Rate, 14 bit Resolution
 - DAC: 4 Channel, 10.0+GSps Sample Rate, 14 bit Resolution
- **ADC/DAC Option #2:** Jariet Technologies Electra-MA
 - ADC: 2 Channel, 64.0GSps Sample Rate, 10 bit Resolution
 - DAC: 2 Channel, 64.0GSps Sample Rate, 10 bit Resolution

SINGLE BOARD COMPUTER (SBC)

- Intel® Xeon® D-1559
- 32G DRAM
- 60GB M.2 SSD/Linux – Standard

APPLICATION DEVELOPMENT

- Standard support delivered with all systems
- Optional full Board Support Package
 - Enables customization of Zynq PS, PL for security
 - Provides fast and robust HDL-based environment



<https://www.annapmicro.com/products/WS3A01-S1/>

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helux Toolkit: MORA software and firmware

Simply put, the helux toolkit eases the development and integration of MORA and VICTORY applications for SOSA™ Technical Standard aligned VPX hardware facilitating SOSA™ adoption within the community. Using the toolkit, hardware vendors, application developers, and system integrators can quickly connect the dots between the MORA/VICTORY interfaces and their hardware while efficiently addressing their customers' SOSA™ requirements and demonstrating the resulting capabilities.

The helux toolkit is a hardware-agnostic, comprehensive solution that provides software implementations of MORA/VICTORY interfaces, HDL modules for framing, filtering and arbitration of MDM/UDP packets, and tools to facilitate end-user interaction and demonstration of SOSA™ hardware. The UI tools include MORA Explorer to enable end-users to visualize and control MORA devices within a domain and MSRP Generator to produce MORA Signal Resource Profiles describing the hardware components' capabilities and position within the overall system.

Sciens Innovations provides system development, integration, and sustainment services backed by an extensive support infrastructure, including an artifact repository, service desk, and SOSA™/MORA experts to streamline the process and provide a solution that reduces risk and market entry costs.

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 @SciensInnovati1

Services and Tools: Software Development Tools



FEATURES

- › Robust software and firmware libraries for MORA 2.4 & 2.5
- › Enables rapid development of client/server applications across VDB and ML2B
- › Integration support for VPX hardware MORA/VICTORY interfaces
- › Tool suite for configuration, interaction, and demonstration of hardware
- › Support portal to request custom features, receive troubleshooting assistance, submit and track bug reports
- › Various licensing options available; package tailored to client-specific needs and hardware platforms

www.sciensinnovations.com/mora-products

Applying a MOSA Strategy for Unmanned Systems (archived webcast)

Sponsored by Elma and Mercury

In 2019, Air Force, Army, and Navy leadership mandated that the U.S. military use a Modular Open Systems Approach (MOSA) for new program designs and refreshes, calling MOSA a “warfighting imperative.” MOSA strategies are now being applied across multiple domains – air, sea, land, space, and electromagnetic spectrum – with unmanned systems a key component in each of those areas. MOSA open architecture initiatives such as The Open Group’s Sensor Open Systems Architecture (SOSA), the Future Airborne Capability Environment (FACE), C5ISR/EW Modular Open Suite of Standards (CMOSS), and others are affecting the hardware and software designs of platforms’ flight controls, ISR payloads, communications, and more.

In this webcast, learn how the military is applying MOSA initiatives and strategies to embedded electronics designs in unmanned platforms.

Watch the webcast: <https://bit.ly/3nLGmcp>

WEBCAST

WATCH MORE WEBCASTS:

<https://militaryembedded.com/webcasts/archive/>



AEROSPACE TechWeek^{com} AMERICAS

8-9 November '22 | Atlanta, USA

MOSA/SOSA/FACE at Aerospace Tech Week Americas

U.S. Air Force, Army, and Navy leaders have mandated that the U.S. military use a Modular Open Systems Approach (MOSA) for new program designs and refreshes. MOSA strategies such as the Future Airborne Capability Environment (FACE) and the Sensor Open Systems Architecture (SOSA) are now being leveraged across multiple defense domains – air, land, sea, space, and spectrum.

The MOSA Conference Track at Aerospace Tech Week Americas will educate attendees on how MOSA strategies and open architecture initiatives are being deployed in military systems and how these approaches enable faster adoption of commercial technology.

MOSA/SOSA/FACE Conference Track – 9th November

Main Conference session topics:

- Open Architectures for Military Aviation Platforms
- MOSA Strategies for Sensor Applications
- Leveraging Commercial Technology for Defense Applications

FREE TO ATTEND WORKSHOPS

MOSA Workshop/Exhibitor Theater – 8th November

The Free to Attend MOSA/SOSA/FACE workshops delivering technology and technical discussions.

MOSA Workshop/Exhibitor Theater topics include:

- MOSA/Open Architectures for Military Systems
- SOSA Technical Standards
- FACE Technical Standards
- Leveraging Commercial Tech for Military Applications



EXHIBITION OPEN 8 & 9th NOV

Latest MOSA/SOSA/FACE Technologies on display at the MOSA Pavilion



Register today for your Free Expo Pass.

Join us at Aerospace Tech Week Americas for the latest updates on MOSA strategies and open architecture initiatives.

Register online at www.aerospacetechnweek.com/americas/register



THE NEXT BIG THING IN RFSoc IS HERE

AND IT'S ONLY 2.5" × 4"

POWERFUL

SMALL

DEPLOYABLE

Models 6001 and 6003 QuartzXM modules enable the rapid integration and deployment of RFSoc technology. And the SWaP-friendly design is ideal for aircraft pods, unmanned vehicles and mast-mounted radars.

A Zynq® UltraScale+™ RFSoc plus a full suite of pre-loaded IP modules, robust Navigator® software, high-speed 100 GigE interfaces and fully integrated hardware from Mercury, formerly Pentek, helps shorten your development time and reduce your design risk.

[Form Factors]

QuartzXM Module
SOSA aligned 3U VPX
3U VPX
SFF platforms
PCIe